120V BOOT, 4A Peak, Half-Bridge Driver with Low Switching Loss

1 FEATURES

- Drives two MOSFETs in high-side and low-side Configuration, 4A Peak Source/Sink Current
- 8V - 20V Wide Supply Voltage Range
- Absolute Maximum Boot and HS Voltage 120V
- Down to -10V Negative Input Voltage Capability
- Absolute Negative Voltage Handling on HS (-20V)
- Fast Propagation Delay: 28ns rising/24ns falling
- 3ns Delay Matching
- Fast Rising and Falling Time: 7ns and 5ns with 1nF capacitor load
- Input interlock
- Under Voltage Lock Out Protection
- Low Quiescent Current: 240uA
- Package with DFN4x4-8L, eSOP-8L, DFN3x3-10L

2 APPLICATIONS

- Power MOSFET Gate Driver
- IGBT Gate Driver
- Switching Power Supply
- Motor Control, Solar Power

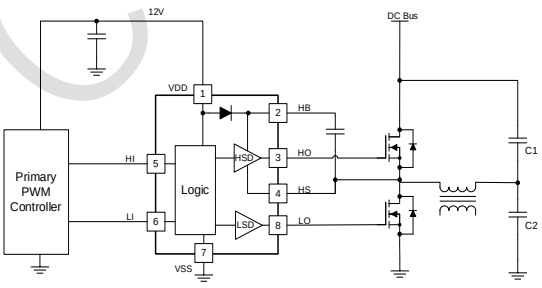
3 ORDERING INFORMATION

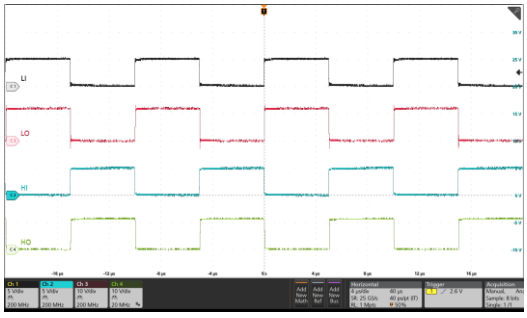
TYPE	MARKING	PACKAGE
GBI7A54NMAR	7A54	DFN4x4-8L
GBI7A54SMAR	7A54	eSOP-8L
GBI7A54NOCR	7A54	DFN3x3-10L

4 DISCRIPTION

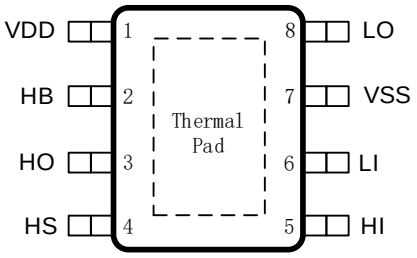
The GBI7A54, provides 4A peak source and sink current along with rail-to-rail driving capability for MOSFET used in half-bridge or synchronous buck configuration. The device features a minimum 24ns input to output propagation delay and 20V power supply rail makes it suitable for high frequency power converter application. The negative input is acceptable down to -10V and the HS pin is able to tolerate significant negative voltage enhance the system noise immunity. The wide input hysteresis is compatible for both TTL and CMOS low voltage logic. The device adopts non-overlap design to avoid the shoot-through between high-side and low-side driver output stage. It operates over a wide temperature range -40°C to 150°C. The GBI7A54 is available in DFN 4 x 4-8L, DFN 3 x 3-10L and eSOP-8L Package.

5 TYPICAL APPLICATIONS

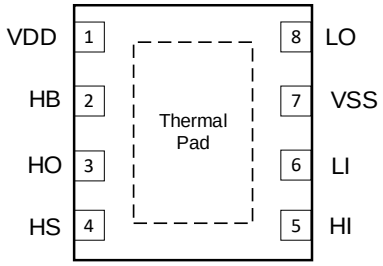




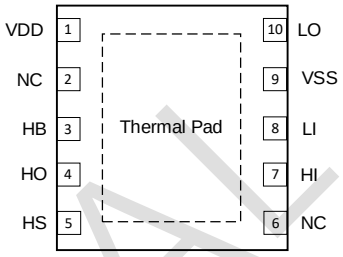
6 PIN CONFIGURATION



Top View (eSOP-8L)



Top View (DFN4x4-8L)



Top View (DFN3x3-10L)

Table 1. PIN CONFIGURATION

PIN OUT			I/O	PIN FUNCTION
PACKAGE	NMA/SMA	NOC		
NAME	NO.	NO.		
VDD	1	1	P	Power Supply to the low-side gate driver. Bypass capacitor is necessary, 4.7uF is recommended.
HB	2	3	I	High side bootstrap supply. The bootstrap diode is integrated, external bootstrap cap is necessary. 100nF is recommended. If external boot diode used, connect cathode of the diode to this pin.
HO	3	4	O	High side output. Connect to high side power MOSFET gate.
HS	4	5	P	High side source connection. Connect to high side power MOSFET source.
HI	5	7	I	High-side input.
LI	6	8	I	Low-side input.
VSS	7	9	-	Negative supply terminal.
LO	8	10	O	Low-side output.
NC	N/A	2,6	-	No connection internally. Pin2 for NC must be floating.
Thermal pad	9	11	-	Must be grounded in PCB layout.

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{DD}	-0.3	20	V
Logic Input	V_{LI}, V_{HI}	-10	20	V
Gate Driver Output	V_{LO} (DC)	V_{SS}-0.3	V_{DD}+0.3	V
	V_{LO} (Pulse<100ns)	V_{SS} -2	V_{DD}+0.3	V
	V_{HO} (DC)	V_{HS}-0.3	V_{HB}+0.3	V
	V_{HO} (Pulse<100ns)	V_{HS}-2	V_{HB}+0.3	V
Voltage on Switching Node HS	V_{HS} (DC)	-1	120	V
	V_{HS} (Pulse<100ns)	-20	120	V
Voltage on HB	V_{HB}	-0.3	120	V
Operating junction temperature	T_J	-40	150	°C
Storage temperature	T_{STG}	-65	150	°C

7.2 ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2000	+2000	V
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (1)	-1000	+1000	V

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

7.3 RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	8	20	V
$V_{LI, HI}$	Input & Enable voltage range	-10	20	V
V_{HB}	Voltage on HB	V_{HS}+8	V_{HS}+20	V
V_{HS}	Voltage on HS (DC)	-1	100	V
	Voltage on HS (Pulse<100ns)	-18	100	V
Voltage slew rate on HS			50	V/ns
T_J	Operating junction temperature	-40	150	°C

7.4 THERMAL INFORMATION

PARAMETER	THERMAL METRIC	DFN-8	eSOP-8L	DFN-10	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	36	40	44	°C/W
$R_{\theta JC}$	Junction to case thermal resistance	41	48	49	°C/W

7.5 ELECTRICAL CHARACTERISTICS

V_{DD}=V_{HB}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

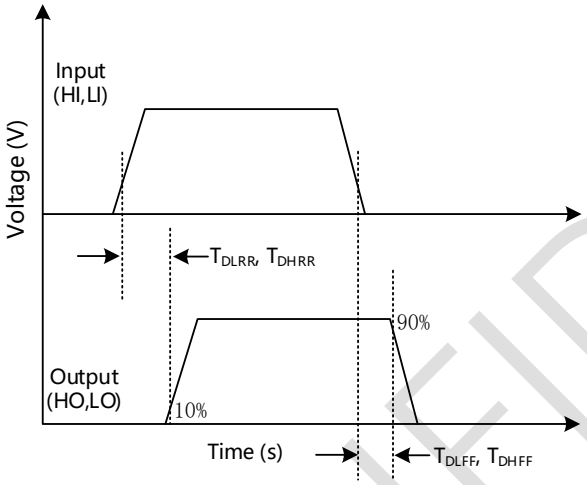
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
I_{DD}	V_{DD} quiescent current	V_{LI}=V_{HI}=0		0.24	0.5	mA
I_{DDO}	V_{DD} operating current	f=500kHz, C_{load}=0		2.2	5	mA
I_{HB}	HB Quiescent current	V_{LI}=V_{HI}=0		0.17	0.4	mA
I_{HBO}	HB Operating current	f=500kHz, C_{load}=0		2.1	4	mA
I_{HBS}	HB to V_{SS} quiescent current			0	50	uA
I_{HBSO}	HB to V_{SS} operating current			1		mA
UNDER VOLTAGE LOCKOUT PROTECTION (UVLO)						
V_{DDR}	V_{DD} rising threshold			7	7.6	V
V_{DDF}	V_{DD} falling threshold		5.9	6.5		V
V_{DDHYS}	V_{DD} threshold hysteresis			0.5		V

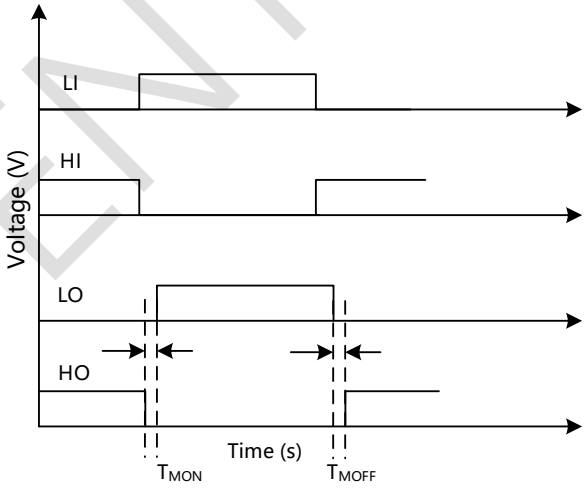
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{HBR}	HB rising threshold with respect to HS		5	6.8	8	V
V_{HBF}	HB falling threshold with respect to HS		5	6.2	7	V
V_{HBHYS}	HB threshold hysteresis			0.6		V
INPUTS						
V_{IH}	input rising threshold		1.9	2.1	2.4	V
V_{IT}	input falling threshold		0.9	1.1	1.3	V
V_{IHYS}	Input voltage Hysteresis			1.0		V
R_{IN}	Input pulldown resistance		100	220	350	kΩ
OUTPUT						
V_{LOL}	Low side low level output voltage	I_{LO}=100mA		0.07	0.4	V
V_{LOH}	Low side high level output voltage	I_{LO}=-100mA, $V_{LOH} = V_{DD} - V_{LO}$		0.1	0.42	V
$I_{LSOURCE}$	Output peak pullup current	V_{LO}=0V		4		A
I_{LSINK}	Output peak pulldown current	V_{LO}=12V		4		A
V_{HOL}	High side low level output voltage	I_{HO}=100mA		0.07	0.4	V
V_{HOH}	High side high level output voltage	I_{HO}=-100mA, V_{HOH}=V_{HB}-V_{HO}		0.1	0.4	V
$I_{HSOURCE}$	Output peak pullup current	V_{HO}=0V		4		A
I_{HSINK}	Output peak pulldown current	V_{HO}=12V		4		A
BOOTSTRAP DIODE						
V_F	Low current forward voltage	I_{VDD-HB}=100uA		0.5	0.8	V
V_{FI}	High current forward voltage	I_{VDD-HB}=100mA		0.9	1.0	V
R_D	Dynamic resistance			0.5	1	Ω
Timing						
T_R	LO, HO Output rising time	C_{Load}=1.0nF		7	13	ns
T_F	LO, HO Output falling time	C_{Load}=1.0nF		5	11	ns
T_{DLFF}	VLI falling to VLO falling		18	24	34	ns
T_{DHFF}	VHI falling to VHO falling		18	24	34	ns
T_{DLRR}	VLI rising to VLO rising		20	28	40	ns
T_{DHRR}	VHI rising to VHO rising		20	28	40	ns

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
DELAY MATCHING						
T_{MON}	From HO being OFF to LO being ON			3	9	ns
T_{MOFF}	From LO being OFF to HO being ON			3	9	ns
$T_{PW,min}$	Minimum input pulse that changes the output			20	36	ns
T_{BST}(1)	Bootstrap diode turn off time			50		ns

(1) Guaranteed by design.

7.6 Timing Diagrams





8 TYPICAL CHARACTERISTICS

V_{DD}=V_{HB}=12V, V_{HS}=V_{VSS}=0V, C_{load}=1nF, T_A= 25°C.

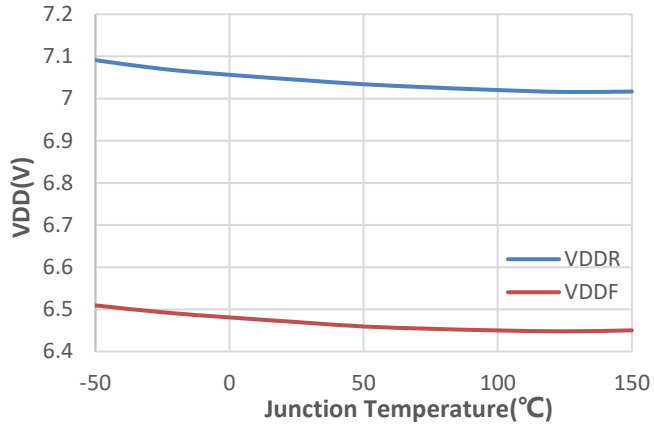


Figure 1. VDD UVLO Vs Temperature

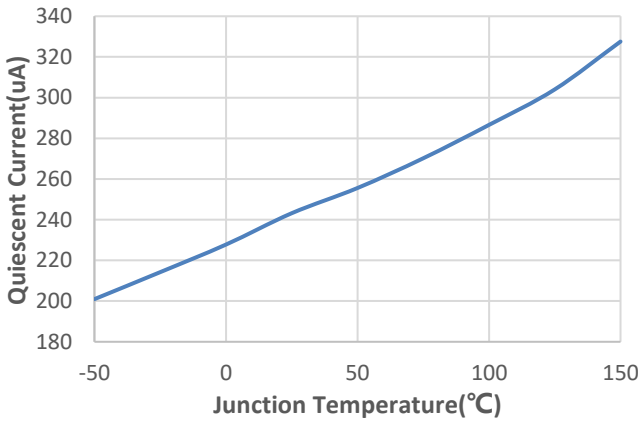


Figure 2. Quiescent Current Vs Temperature

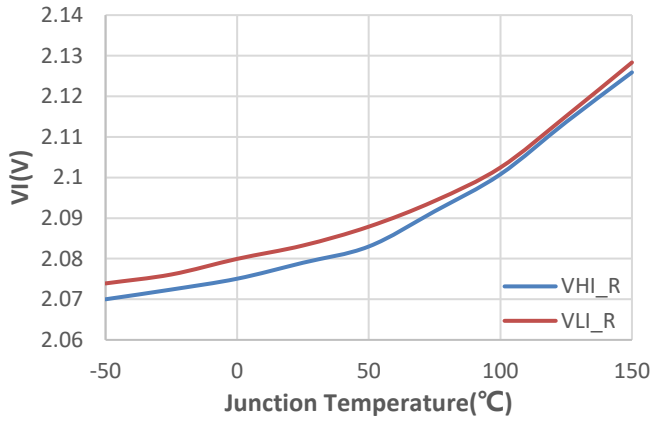


Figure 3. Input Rising Threshold Vs Temperature

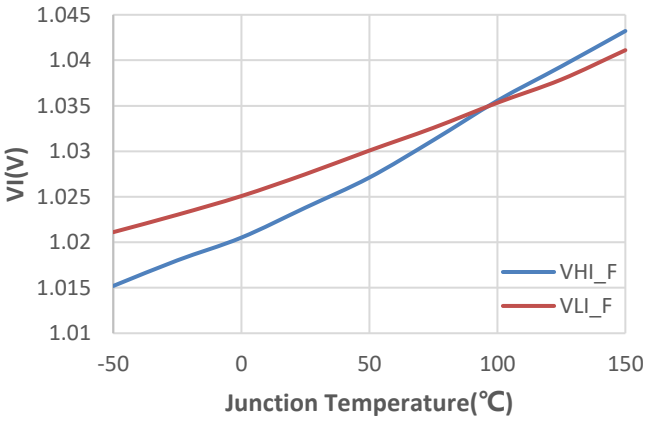


Figure 4. Input Falling Threshold Vs Temperature

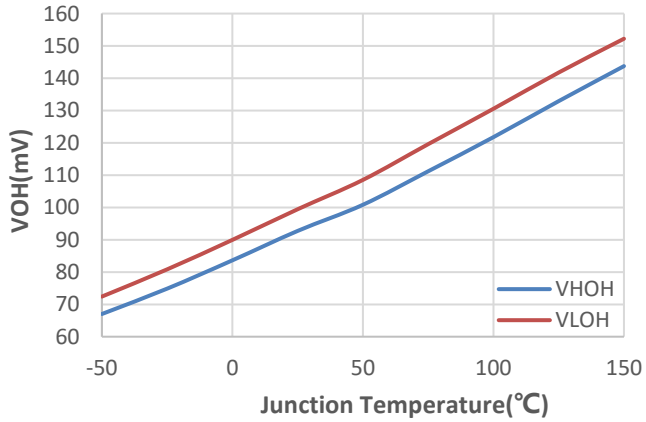


Figure 5. Output High Voltage Vs Temperature

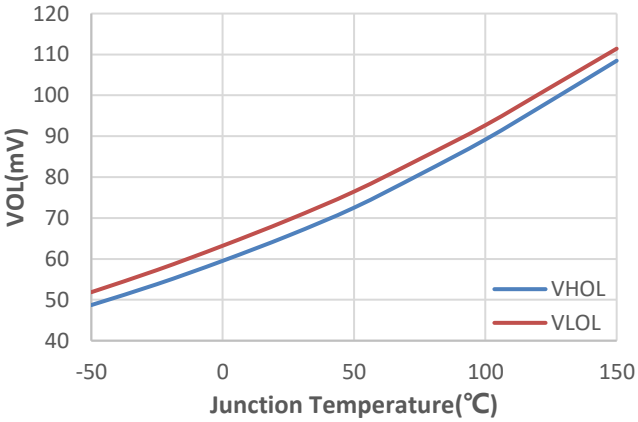


Figure 6. Output Low Voltage Vs Temperature

9 FUNCTIONAL BLOCK DIAGRAM

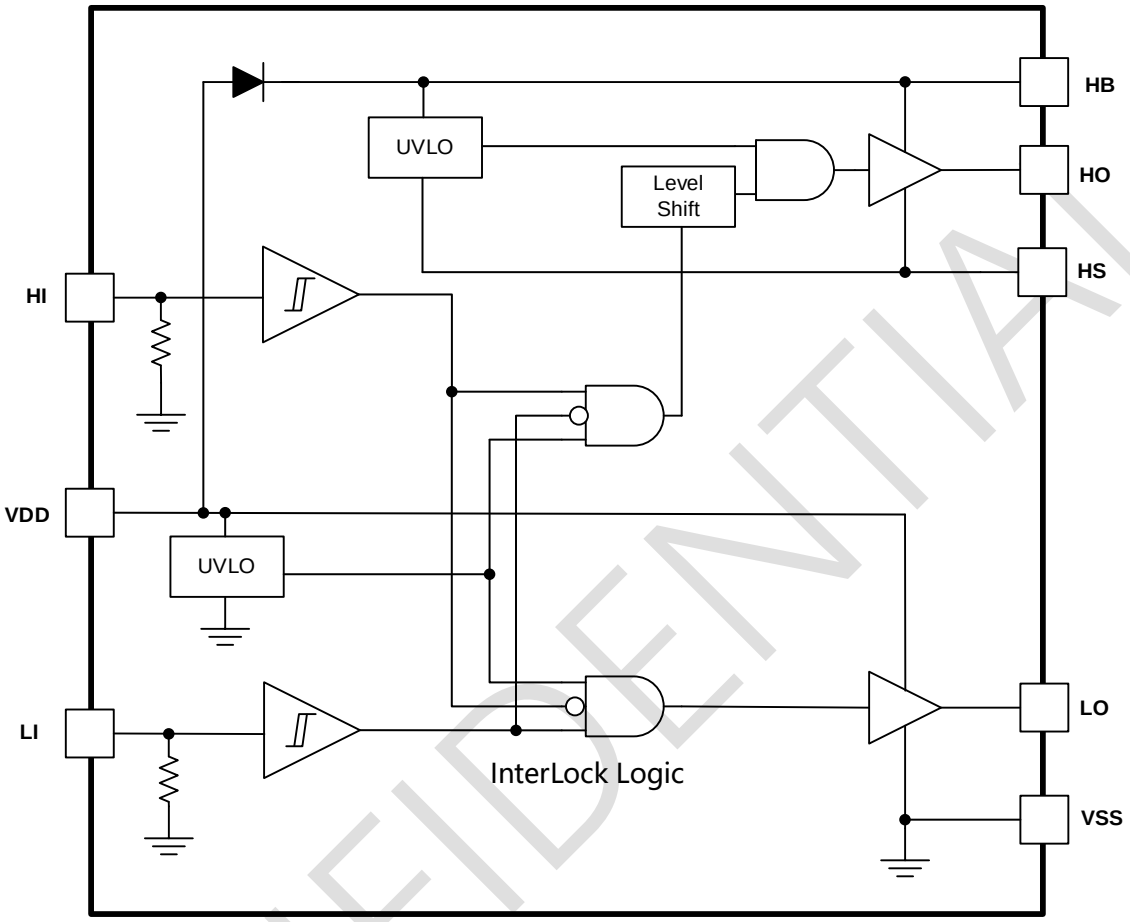


Figure 7. GBI7A54 Block Diagram

10 DISCRIPTION

10.1 Overview

The GBI7A54 is a high-voltage gate driver designed to drive both the high-side and the low-side N-channel FETs in a synchronous buck or a half-bridge configuration. The two outputs are independently controlled by two TTL-compatible input signals. The floating high-side driver is capable of working with HS voltage up to 120V with respect to VSS. A 120V bootstrap diode is integrated to charge high-side gate drive bootstrap capacitor.

Undervoltage lockout (UVLO) is provided on both the low-side and the high-side power rails. The driver also has input interlock functionality, which shuts off both the outputs when the two inputs have overlap.

10.2 VDD Power Supply

The GBI7A54 operates under a supply voltage range between 8V to 20V. It' s recommended to put two VDD bypass capacitor in parallel to prevent noise problems on supply VDD. It has to put a 0.1uF SMT ceramic capacitor as close as possible between the VDD pin and the GND pin. To avoid the unexpected VDD glitch, a large capacitor (ex. 1uF or 10uF) with relatively low ESR must be connected in parallel with that 0.1uF capacitor. This parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

10.3 Under Voltage Lock Out (UVLO)

In GBI7A54, Both the high-side and the low-side driver stages include UVLO protection circuitry which monitors the supply voltage (VDD) and the bootstrap capacitor voltage (VHB–VHS). The UVLO circuit inhibits each output until sufficient supply voltage is available to turn on the external MOSFETs. The built-in UVLO hysteresis prevents chattering during supply voltage variations. When the supply voltage is applied to the VDD pin of the device, both the outputs are held low until VDD exceeds the UVLO threshold, typically 7V. UVLO condition on the bootstrap capacitor (VHB–VHS) disables only the high- side output (HO).

Table 2. GBI7A54 VDD UVLO Device Logic

Condition	HI	LI	HO(1)	LO(2)
V_{DD}-V_{SS} < V_{DDR} during device start-up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L
V_{DD}-V_{SS}<V_{DDR}-V_{DDHYS} after device start-up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L

(1) HO is measured with respect to HS.

(2) LO is measured with respect to VSS.

Table 3. HB UVLO Device Logic Operation

Condition	HI	LI	HO(1)	LO(2)
V_{HB-HS} < V_{HBR} during device start-up	H	L	L	L
	L	H	L	H
	H	H	L	L
	L	L	L	L
V_{HB-HS}<V_{HBR}-V_{HBHYS} after device start-up	H	L	L	L
	L	H	L	H
	H	H	L	L
	L	L	L	L

(1) HO is measured with respect to HS.

(2) LO is measured with respect to VSS.

10.4 Input Stage

The GBI7A54 input is compatible with TTL logic which is independent of the VDD supply voltage. The typical threshold is 2.1V (high) and 1.1V (low), which makes the device easily driven by PWM control signals derived from 3.3V and 5V digital power-controller devices. The device features wider hysteresis compared to typical threshold of 0.5V which offers enhanced noise immunity. It also implements tight control of the input threshold voltage that ensures stable operation across temperature. The low input capacitance on the input pins increases switching speed and reduces the propagation delay.

The two inputs operate independently, with an exception that both outputs will be pulled low when both inputs are high or overlap. The independence allows for full control of two outputs compared to the gate drivers that have a single input. The device has input interlock or cross-conduction protection. Whenever both the inputs are high, the internal logic turns both the outputs off. Once the device is in shoot-through mode, when one of the inputs goes low, the outputs follow the input logic. There is no built-in dead-time due to the interlock feature. Any noise on the input that could cause the output to shoot-through will be filtered by this feature and the system stays protected. Because the inputs are independent of supply voltage, they can be connected to outputs of either digital controller or analog controller. Inputs can accept wide slew rate signals and input can withstand negative voltage to increase the robustness.

Small filter at the inputs of the driver further improves system robustness in noise prone applications. The inputs have internal pull-down resistors with typical value of 220kΩ. Thus, when the inputs are floating, the outputs are held low.

10.5 Interlock

The two inputs operate independently, with an exception that both outputs will be pulled low when both inputs are high or overlap. The independence allows for full control of two outputs compared to the gate drivers that have a single input. The device has input interlock or cross-conduction protection. Whenever both the inputs are high, the internal logic turns both the outputs off. Once the device is in shoot-through mode, when one of the inputs goes low, the outputs follow the input logic. There is no built-in dead-time due to the interlock feature. Any noise on the input that could cause the output to shoot-through will be filtered by this feature and the system stays protected. Because the inputs are independent of supply voltage, they can be connected to outputs of either digital controller or analog controller. Inputs can accept wide slew rate signals and input can withstand negative voltage to increase the robustness. Small filter at the inputs of the driver further improves system robustness in noise prone applications.

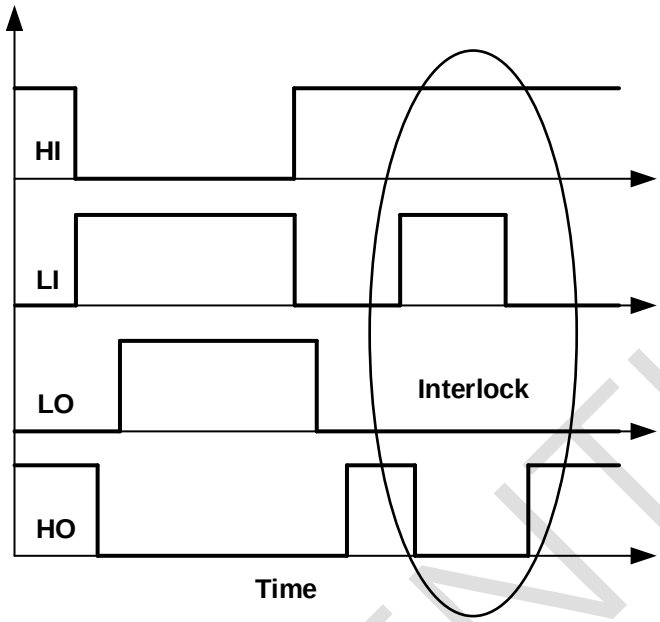


Figure 8. Interlock or Input Shoot-through Protection

10.6 Output Stage

The output stages are the interface from level shifter output to the power MOSFETs in the power train. High slew rate, low resistance, and high peak current capability of both outputs allow for efficient switching of the power MOSFETs. The low-side output stage is referenced to VSS and the high-side is referenced to HS. The device output stages are robust to handle harsh environment, such as –2V transient for 100 ns. The device can also sustain positive transients on the outputs. The device output stages feature a pull-up structure which delivers the highest peak source current when it is needed, during the Miller plateau region of the power switch turn on transition. The output pull-up and pull-down structure of the device is totem pole NMOS-PMOS structure.

10.7 Negative Voltage Transients on Switching Node HS

In most applications, the body diode of the external low-side power MOSFET clamps the HS node to ground. In some situations, board capacitances and inductances can cause the HS node to transiently swing several volts below ground, before the body diode of the external low-side MOSFET clamps this swing. When used in conjunction with the GBI7A54, the HS node can swing below ground as long as specifications are not violated and conditions mentioned in this section are followed, please refer to section 7.3 recommended operating conditions. As listed in 7.3 recommended operating conditions, the HB to HS voltage should be 20V or less.

HS must always be at a lower potential than HO. Pulling HO more negative than specified conditions (refer to 7.1) can activate parasitic transistors which may result in excessive current flow from the HB supply VDD. This may result in damage to the device. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and VSS to protect the device from this type of transient. The diode must be placed as close to the device pins as possible in order to be effective.

Generally, when HS swings negative, HB follows HS instantaneously and therefore the HB to HS voltage does not significantly overshoot. A Low ESR bypass capacitors from HB to HS and from VDD to VSS are essential for proper operation of the gate driver device. The capacitor should be located at the leads of the device to minimize series inductance. The peak currents from LO and HO can be quite large, any series inductances with the bypass capacitor causes voltage ringing at the leads of the device must be avoided for reliable operation. Based on application board design and other operating parameters.

10.8 Negative Voltage Transients on Inputs and Outputs

Along with HS pin, other pins such as inputs, HI and LI, might also transiently swing below ground. To accommodate such operating conditions , GBI7A54 input pins are capable of handling absolute maximum of -10V. As explained before, based on the layout and other design constraints, sometimes the outputs, HO and LO, might also see negative transient voltages for short durations. Therefore, GBI7A54 gate driver is designed to handle -2V/100 ns transients on output pins, HO and LO.

10.9 Device Functional Modes

When the device is enabled, the device operates in normal mode and UVLO mode. See Section 10.3 for more information on UVLO operation mode. In normal mode when the VDD and VHB–HS are above UVLO threshold, the output stage is dependent on the states of the HI and LI pins. The output HO and LO will be low if input state is floating.

Table 4. Input/Output Logic in Normal Mode of Operation

HI	LI	HO(1)	LO(2)
H	H	L	L
L	H	L	H
H	L	H	L
L	L	L	L
Floating	L	L	L
Floating	H	L	H
L	Floating	L	L
H	Floating	H	L

(1) HO is measured with respect to pin HS.

(2) LO is measured with respect to pin VSS.

11 APPLICATION INFORMATION

11.1 Typical Application

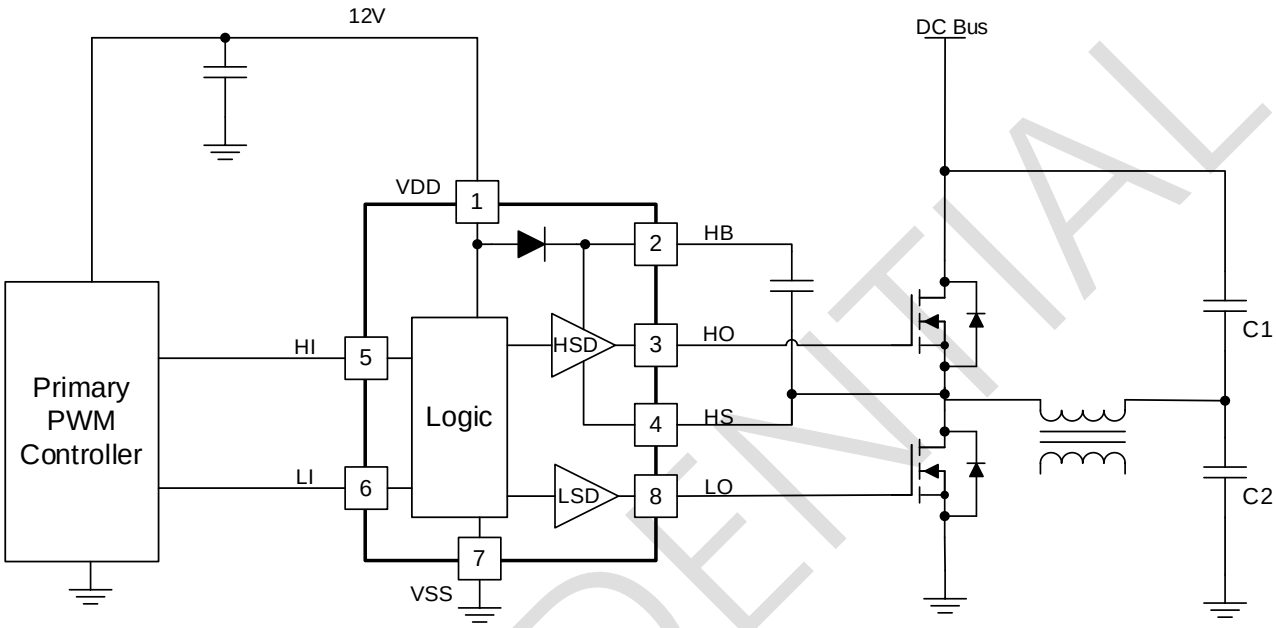


Figure 9. Typical Configuration

11.2 Driver Power Dissipation

Generally, the power dissipation depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The GBI7A54 is designed with very low quiescent currents and internal logic to eliminate any output-stage shoot-through.

The power loss of GBI7A54 caused by pure capacitive load is:

$$P_G = C_{Load} * V_{DD}^2 * f_{SW} \quad (1)$$

Where

- V_{DD} is supply voltage
- C_{Load} is the output capacitance
- f_{SW} is the switching frequency

This equation (1) is also able to be adopted to calculate the switching load of power MOSFET, where gate charge Qg determines the capacitor charges.

$$Q_g = C_{LOAD} \times V_{DD} \quad (2)$$

Normally power device manufacturers provide specifications with the typical and maximum Qg, in nC, to switch the device under specified conditions.

$$P_G = Q_g * V_{DD} * f_{SW} \quad (3)$$

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

Sometimes, circuit designers put a resistor R_{GATE} between the driver output pin and the gate terminal of power device to slow down the power device transition. As a result, the ringing caused by the parasitic inductor is eliminated. The power dissipation of the driver shows as below:

$$P_G = \frac{1}{2} * Q_g * V_{DD} * f_{SW} * \left(\frac{R_L}{R_L + R_{GATE}} + \frac{R_H}{R_H + R_{GATE}}\right) \quad (4)$$

Where

- R_H is the equivalent pull up resistance of GBI7A54
- R_L is the equivalent pull-down resistance of GBI7A54
- R_{GATE} is the gate resistance between driver output and gate of power device.

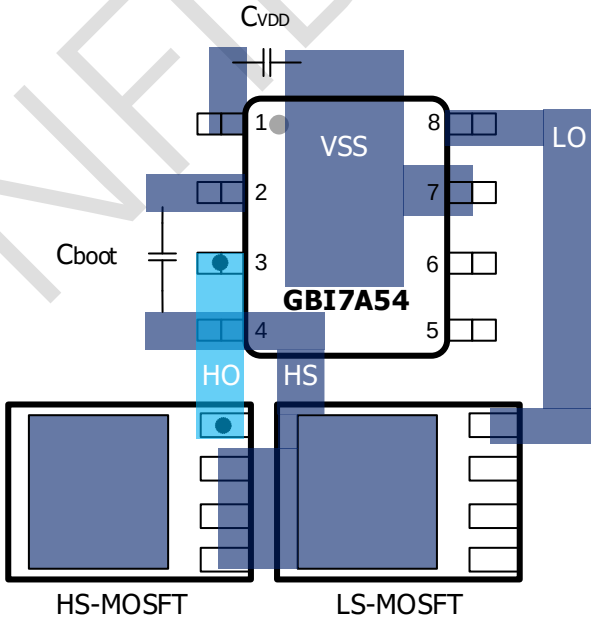
12 LAYOUT

12.1 Layout Guideline

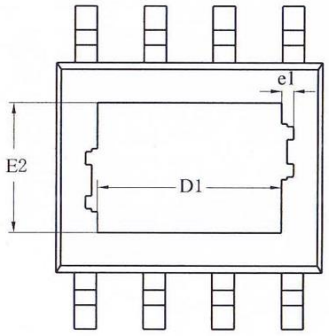
Layout is critical for proper operation. Please follow the layout guidelines.

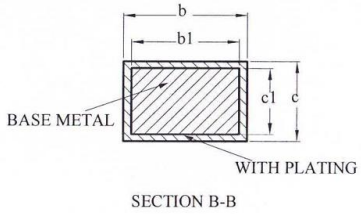
1. Minimize the parasitic inductance between the source of the High-side MOSFET and the drain of the Low-side MOSFET, to avoid the large negative transient on switch node HS.
2. Place the gate driver as close as possible to the MOSFET, and trace the driver output signal as short as possible to the gate of both the High-side and Low-side MOSFET.
3. Place the bypass input capacitor with low ESR as close as possible between the VDD and VSS. The bypassing loop from VDD terminal to the VSS should be as short as possible.
4. Place the bootstrap cap as close as possible between the HB and HS. The capacitor should be located at the leads of the device to minimize series inductance.
5. A low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the High-side MOSFET drain and VSS, to avoid the large transient voltage on the drain of the High-side MOSFET.

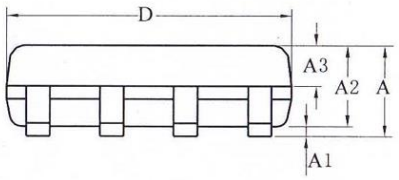
12.2 Layout Example

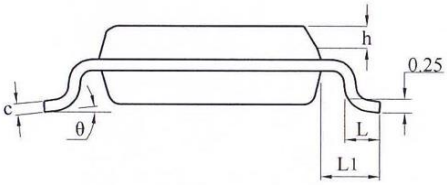


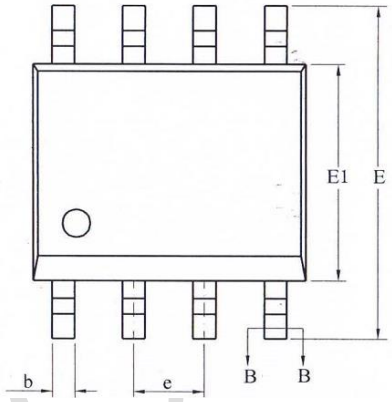
PACKAGE INFORMATION - eSOP-8L









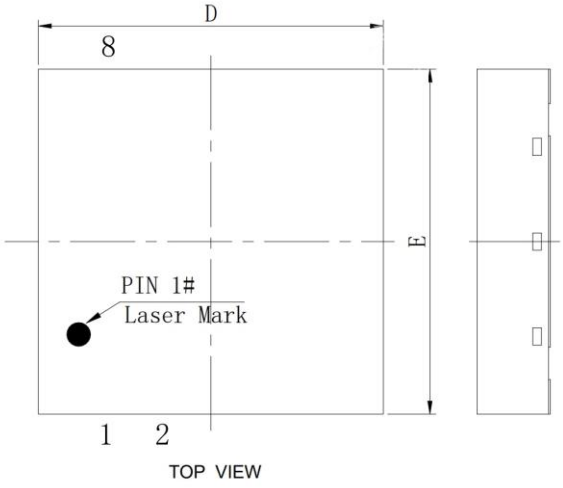


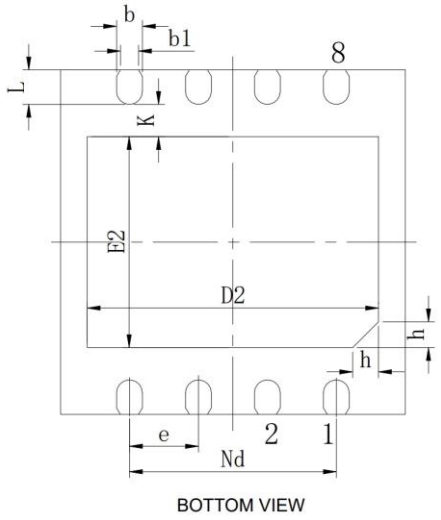
Top View

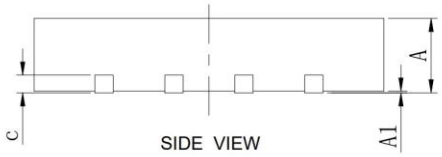
LF Size	D1	E2	e1
95*130	3.1	2.21	0.10REF

Symbol	Millimeter		
	Min	Nor	Max
A	-	-	1.65
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	0.60	0.80
L1	1.05REF		
θ	0	-	8°

PACKAGE INFORMATION – DFN4x4-8L

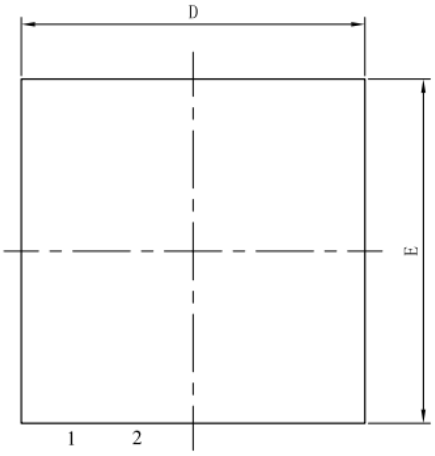




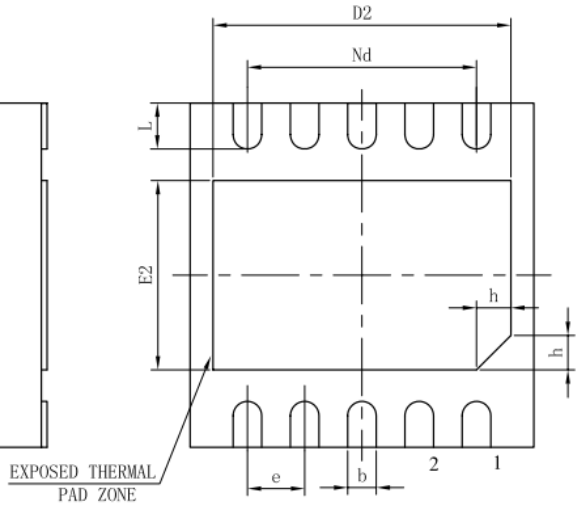


Symbol	Millimeter		
	Min	Nor	Max
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.25	0.30	0.35
b1	0.21REF		
c	0.203REF		
D	3.90	4.00	4.10
D2	3.28	3.38	3.48
Nd	2.40BSC		
e	0.80BSC		
E	3.90	4.00	4.10
E2	2.35	2.45	2.55
L	0.35	0.40	0.45
K	0.375REF		
h	0.25	0.30	0.35

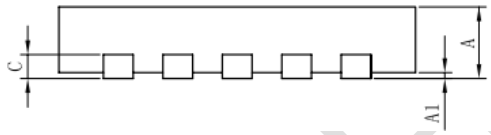
PACKAGE INFORMATION – DFN3x3-10L



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Millimeter		
	Min	Nor	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
Nd	2.00BSC		
e	0.50BSC		
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
L	0.30	0.40	0.50
h	0.20	0.25	0.30