

SBOS313B − AUGUST 2004 − REVISED NOVEMBER 2004

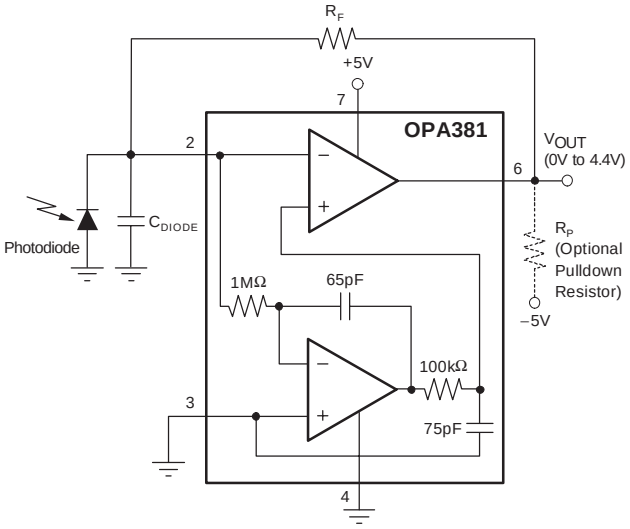
Precision, Low Power, 18MHz Transimpedance Amplifier

FEATURES

- OVER 250kHz TRANSIMPEDANCE BANDWIDTH
- DYNAMIC RANGE: 5 Decades
- EXCELLENT LONG-TERM STABILITY
- LOW VOLTAGE NOISE: 10nV/$\sqrt{\text{Hz}}$
- BIAS CURRENT: 3pA
- OFFSET VOLTAGE: 25μV (max)
- OFFSET DRIFT: 0.1μV/°C (max)
- GAIN BANDWIDTH: 18MHz
- QUIESCENT CURRENT: 800μA
- FAST OVERLOAD RECOVERY
- SUPPLY RANGE: 2.7V to 5.5V
- SINGLE AND DUAL VERSIONS
- *Micro*PACKAGE: DFN-8, MSOP-8

APPLICATIONS

- PRECISION I/V CONVERSION
- PHOTODIODE MONITORING
- OPTICAL AMPLIFIERS
- CAT-SCANNER FRONT-END
- PHOTO LAB EQUIPMENT



DESCRIPTION

The OPA381 family of transimpedance amplifiers provides 18MHz of Gain Bandwidth (GBW), with extremely high precision, excellent long-term stability, and very low 1/f noise. The OPA381 features an offset voltage of 25μV (max), offset drift of 0.1μV/°C (max), and bias current of 3pA. The OPA381 far exceeds the offset, drift, and noise performance that conventional JFET op amps provide.

The signal bandwidth of a transimpedance amplifier depends largely on the GBW of the amplifier and the parasitic capacitance of the photodiode, as well as the feedback resistor. The 18MHz GBW of the OPA381 enables a transimpedance bandwidth of > 250kHz in most configurations. The OPA381 is ideally suited for fast control loops for power level measurement on an optical fiber.

As a result of the high precision and low-noise characteristics of the OPA381, a dynamic range of 5 decades can be achieved. This capability allows the measurement of signal currents on the order of 10nA, and up to 1mA in a single I/V conversion stage. In contrast to logarithmic amplifiers, the OPA381 provides very wide bandwidth throughout the full dynamic range. By using an external pulldown resistor to –5V, the output voltage range can be extended to include 0V.

The OPA381 and OPA2381 are both available in MSOP-8 and DFN-8 (3mm x 3mm) packages. They are specified from –40°C to +125°C.

OPA381 RELATED DEVICES

PRODUCT	FEATURES
OPA380	90MHz GBW, 2.7V to 5.5V Supply Transimpedance Amplifier
OPA132	16MHz GBW, Precision FET Op Amp ±15V
OPA300	150MHz GBW, Low-Noise, 2.7V to 5.5V Supply
OPA335	10μV V_{OS}, Zero-Drift, 2.5V to 5V Supply
OPA350	500μV V_{OS}, 38MHz, 2.5V to 5V Supply
OPA354	100MHz GBW CMOS, RRIO, 2.5V to 5V Supply
OPA355	200MHz GBW CMOS, 2.5V to 5V Supply
OPA656/7	230MHz, Precision FET, ±5V

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ABSOLUTE MAXIMUM RATINGS(1)

Voltage Supply	+7V
Signal Input Terminals(2), Voltage	(V−) −0.5V to (V+) + 0.5V
Current	±10mA
Short-Circuit Current(3)	Continuous
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
OPA381 ESD Rating (Human Body Model)	2000V
OPA2381 ESD Rating (Human Body Model)	1500V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground; one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

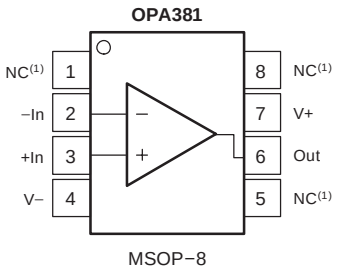
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA381	MSOP-8	DGK	−40°C to +125°C	A64	OPA381AIDGKT	Tape and Reel, 250
					OPA381AIDGKR	Tape and Reel, 2500
OPA381	DFN-8	DRB	−40°C to +125°C	A65	OPA381AIDRBT	Tape and Reel, 250
					OPA381AIDRBR	Tape and Reel, 3000
OPA2381	MSOP-8	DGK	−40°C to +125°C	A62	OPA2381AIDGKT	Tape and Reel, 250
					OPA2381AIDGKR	Tape and Reel, 2500
OPA2381	DFN-8	DRB	−40°C to +125°C	A63	OPA2381AIDRBT	Tape and Reel, 250
					OPA2381AIDRBR	Tape and Reel, 3000

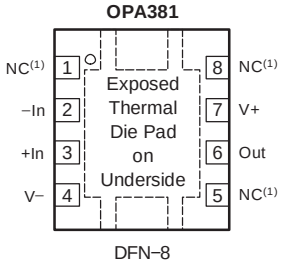
(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

PIN ASSIGNMENTS

Top View

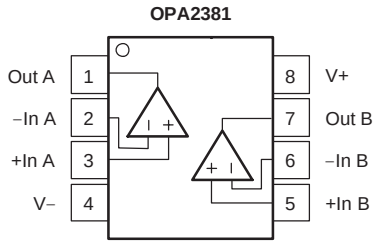


MSOP−8

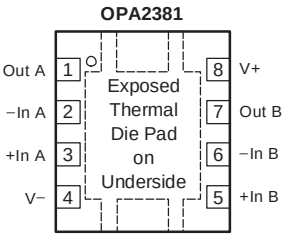


DFN−8

NOTE: (1) NC indicates no internal connection.



MSOP−8



DFN−8

ELECTRICAL CHARACTERISTICS: V_S = +2.7V to +5.5V

Boldface limits apply over the temperature range, **T_A = −40°C to +125°C**.

All specifications at T_A = +25°C, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		CONDITION	OPA381 MIN	OPA381 TYP	OPA381 MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = +5V, V_{CM} = 0V		7	25	µV
Drift	**dV_{OS}/dT**			**0.03**	**0.1**	**µV/°C**
vs Power Supply	PSRR	V_S = +2.7V to +5.5V, V_{CM} = 0V		3.5	20	µV/V
Over Temperature		**V_S = +2.7V to +5.5V, V_{CM} = 0V**			**20**	**µV/V**
Long-Term Stability(1)				See Note (1)		
Channel Separation, dc				1		µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = V_S/2		3	±50	pA
Over Temperature				See Typical Characteristics		
Input Offset Current	I_{OS}	V_{CM} = V_S/2		6	±100	pA
NOISE						
Input Voltage Noise, f = 0.1Hz to 10Hz	e_n	V_S = +5V, V_{CM} = 0V		3		μV_{PP}
Input Voltage Noise Density, f = 10kHz	e_n	V_S = +5V, V_{CM} = 0V		70		nV/√Hz
Input Voltage Noise Density, f > 1MHz	e_n	V_S = +5V, V_{CM} = 0V		10		nV/√Hz
Input Current Noise Density, f = 10kHz	i_n	V_S = +5V, V_{CM} = 0V		20		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		V−		(V+) − 1.8V	V
Common-Mode Rejection Ratio	**CMRR**	**V_S = +5V, (V−) < V_{CM} < (V+) − 1.8V**	**95**	**110**		**dB**
INPUT IMPEDANCE						
Differential Capacitance				1		pF
Common-Mode Resistance and Capacitance				10^{13} || 2.5		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	**A_{OL}**	**0.05V < V_O < (V+) − 0.6V, V_{CM} = V_S/2, V_S = 5V**	**110**	**135**		**dB**
		0V < V_O < (V+) − 0.6V, V_{CM} = 0V, R_P = 10kΩ to −5V(2), V_S = 5V	**106**	**135**		**dB**
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			18		MHz
Slew Rate	SR	G = +1		12		V/µs
Settling Time, 0.0015%(3)		V_S = +5V, 4V Step, G = +1, OPA381		7		µs
Settling Time, 0.003%(3)		V_S = +5V, 4V Step, G = +1, OPA2381		7		µs
Overload Recovery Time(4), (5)		V_{IN} • G = > V_S		200		ns
OUTPUT						
Voltage Output Swing from Positive Rail		**R_L = 10kΩ**		**400**	**600**	**mV**
Voltage Output Swing from Negative Rail		**R_L = 10kΩ**		**30**	**50**	**mV**
Voltage Output Swing from Positive Rail		**R_P = 10kΩ to −5V(2)**		**400**	**600**	**mV**
Voltage Output Swing from Negative Rail		**R_P = 10kΩ to −5V(2)**		**−20**	**0**	**mV**
Output Current	I_{OUT}			10		mA
Short-Circuit Current	I_{SC}			20		mA
Capacitive Load Drive	C_{LOAD}			See Typical Characteristics		
Open-Loop Output Impedance	R_O	F = 1MHz, I_O = 0		250		Ω
POWER SUPPLY						
Specified Voltage Range	V_S		2.7		5.5	V
Quiescent Current (per amplifier)	I_Q	I_O = 0A		0.8	1	mA
Over Temperature					**1.1**	**mA**
TEMPERATURE RANGE						
Specified and Operating Range			−40		+125	°C
Storage Range			−65		+150	°C
Thermal Resistance	θ_{JA}					
MSOP-8				150		°C/W
DFN-8				65		°C/W

(1) High temperature operating life characterization of zero-drift op amps applying the techniques used in the OPA381 have repeatedly demonstrated randomly distributed variation approximately equal to measurement repeatability of 1µV. This consistency gives confidence in the stability and repeatability of these zero-drift techniques.

(2) Tested with output connected only to R_P, a pulldown resistor connected between V_{OUT} and −5V, as shown in Figure 3. See also ***Applications*** section, *Achieving Output Swing to Negative Rail.*

(3) Transimpedance frequency of 250kHz.

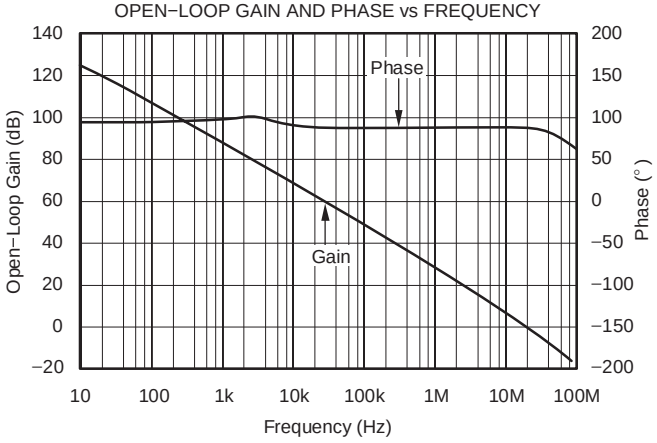
(4) Time required to return to linear operation.

(5) From positive rail.

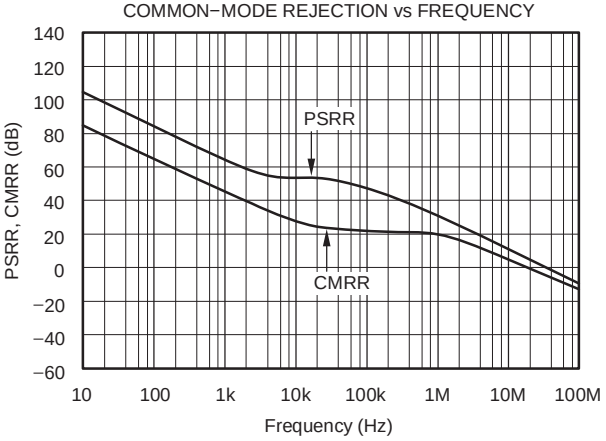
TYPICAL CHARACTERISTICS: V_S = +2.7V to +5.5V

All specifications at T_A = +25°C, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

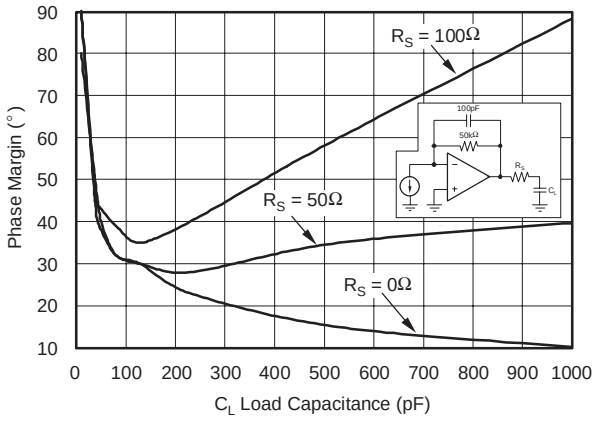
OPEN−LOOP GAIN AND PHASE vs FREQUENCY



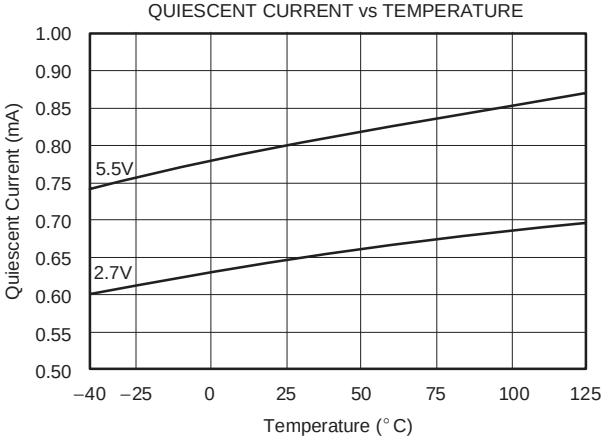
POWER−SUPPLY REJECTION RATIO AND COMMON−MODE REJECTION vs FREQUENCY



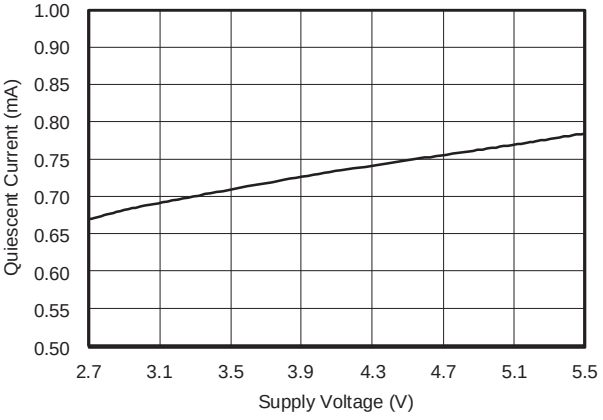
PHASE MARGIN vs LOAD CAPACITANCE



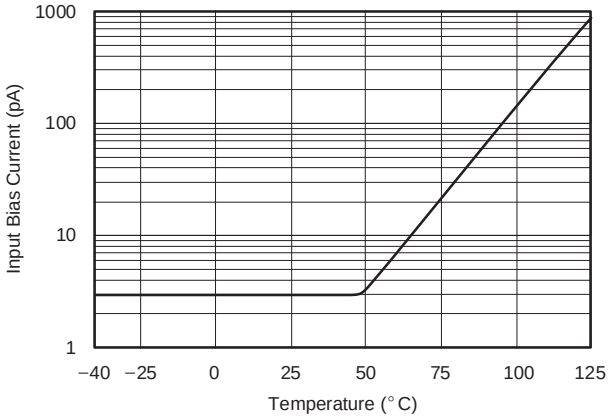
QUIESCENT CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs SUPPLY VOLTAGE



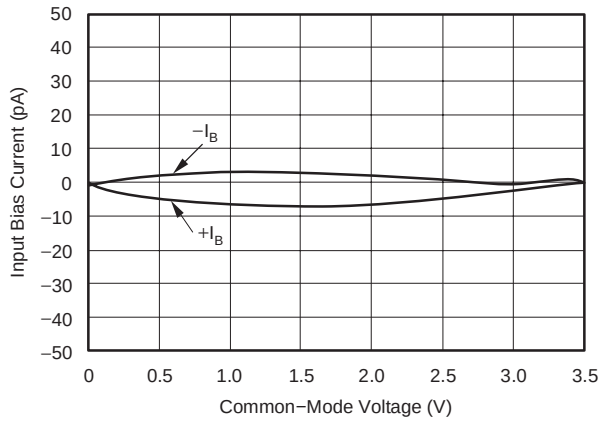
INPUT BIAS CURRENT vs TEMPERATURE



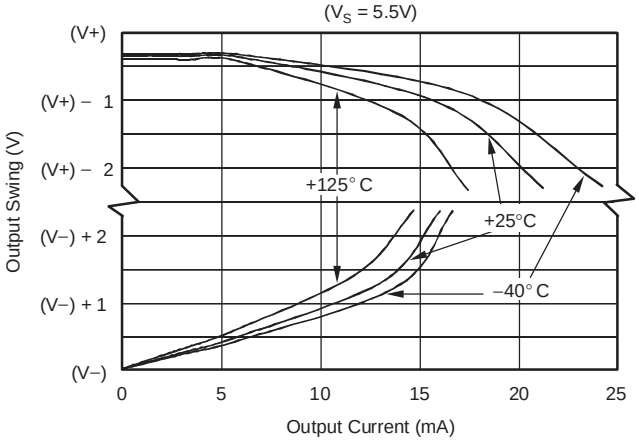
TYPICAL CHARACTERISTICS: V_S = +2.7V to +5.5V (continued)

All specifications at T_A = +25°C, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

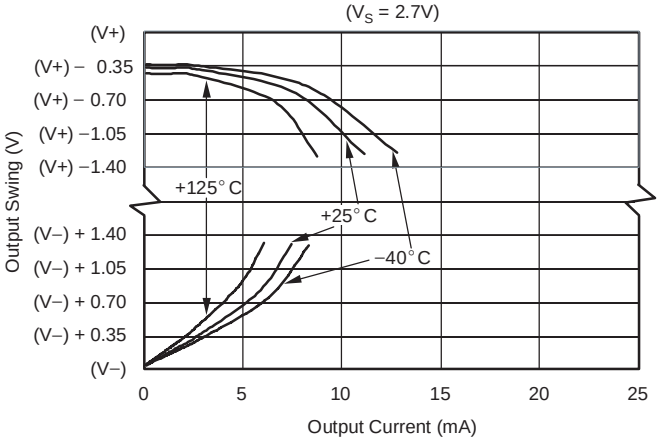
INPUT BIAS CURRENT
vs COMMON−MODE VOLTAGE



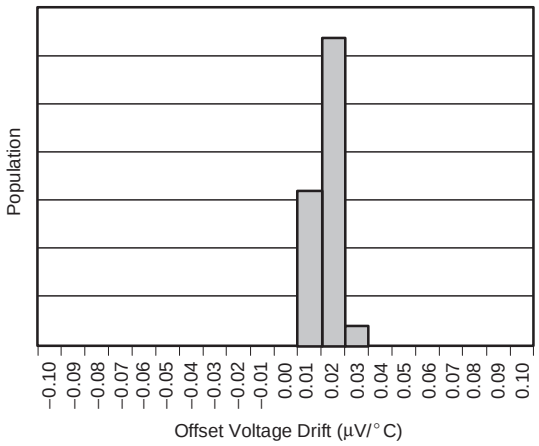
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT
(V_S = 5.5V)



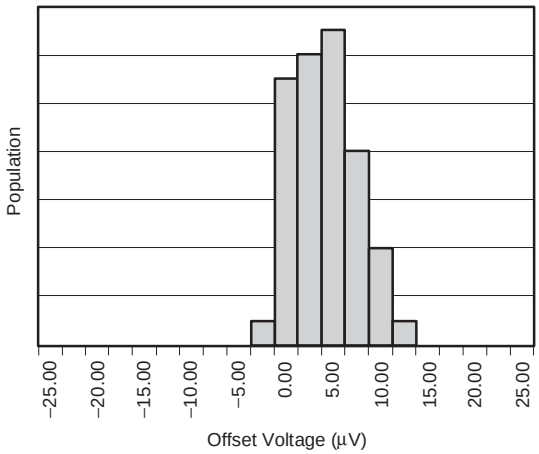
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT
(V_S = 2.7V)



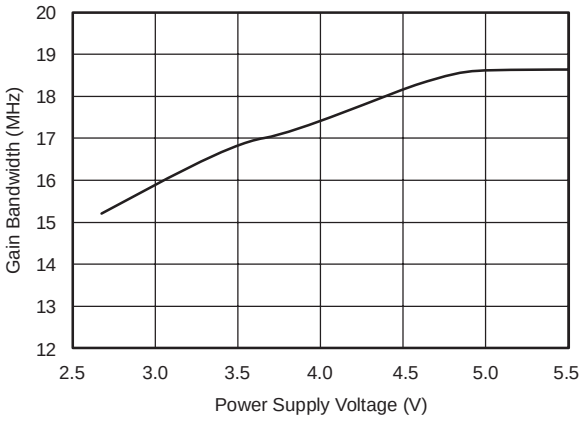
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



OFFSET VOLTAGE PRODUCTION DISTRIBUTION



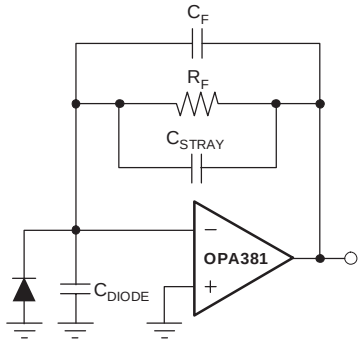
GAIN BANDWIDTH vs POWER SUPPLY VOLTAGE



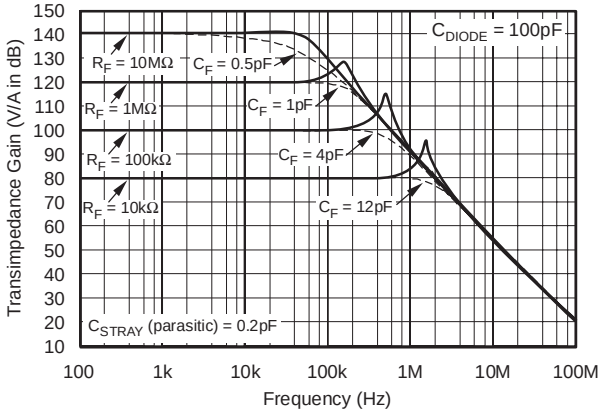
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All specifications at T_A = +25°C, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

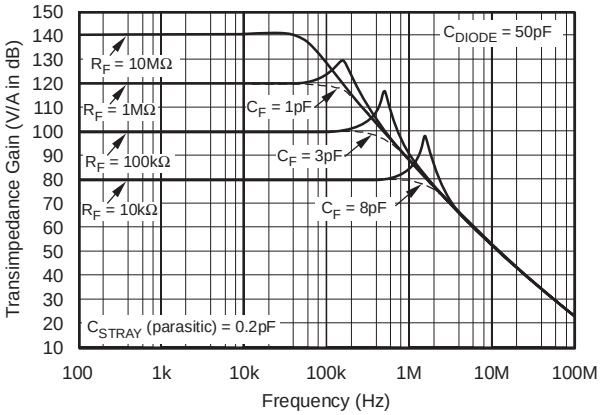
Circuit for *Transimpedance Amplifier Characteristic* curves on this page.



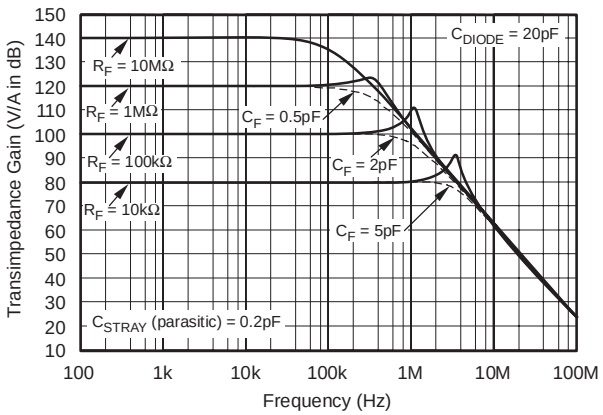
TRANSIMPEDANCE AMP CHARACTERISTIC



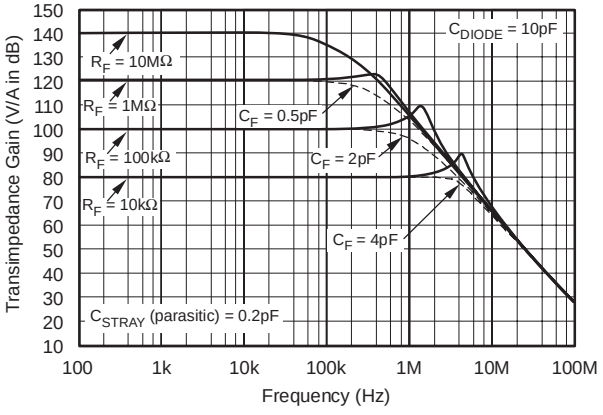
TRANSIMPEDANCE AMP CHARACTERISTIC



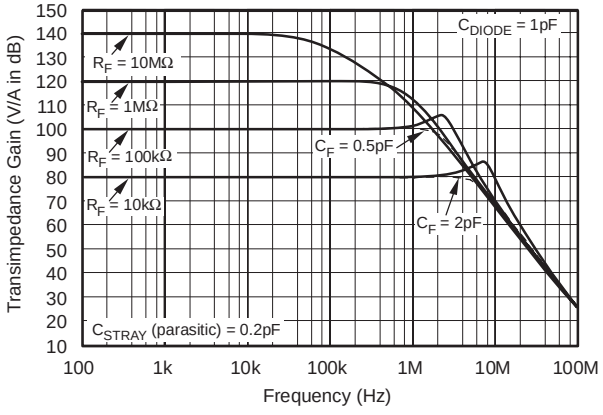
TRANSIMPEDANCE AMP CHARACTERISTIC



TRANSIMPEDANCE AMP CHARACTERISTIC



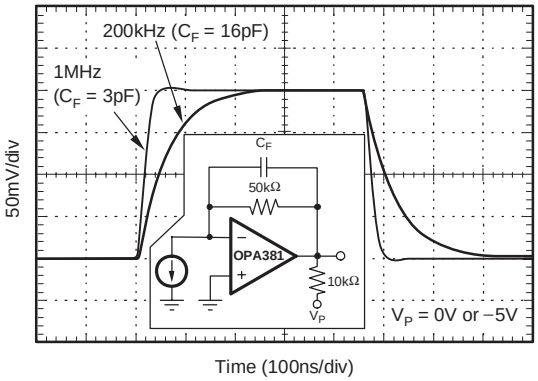
TRANSIMPEDANCE AMP CHARACTERISTIC



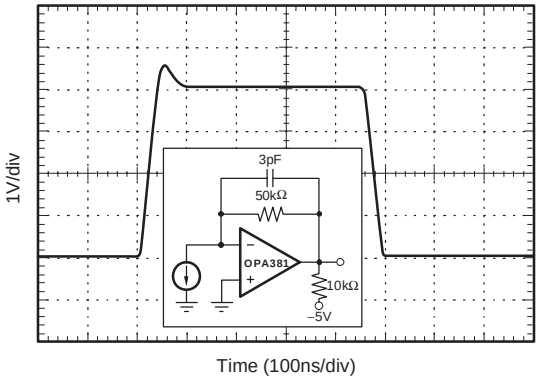
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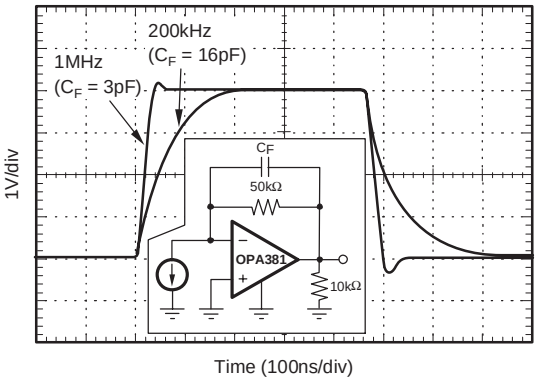
SMALL−SIGNAL STEP RESPONSE
(with or without pull−down)



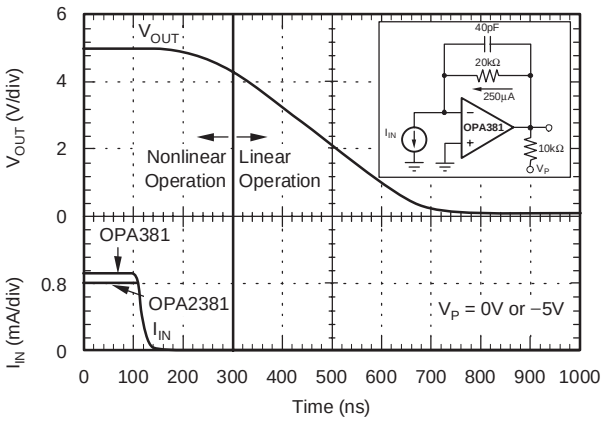
LARGE−SIGNAL STEP RESPONSE
(with pull−down)



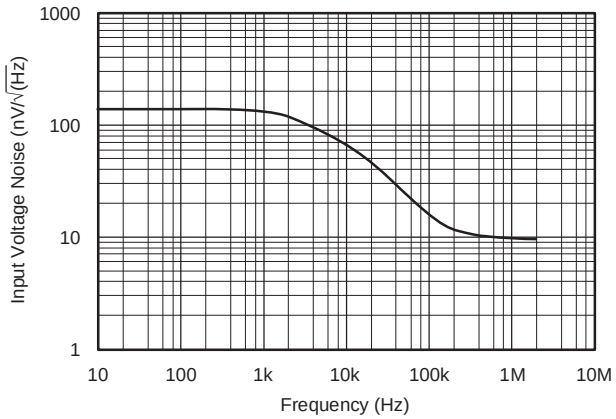
LARGE−SIGNAL STEP RESPONSE
(without pull−down)



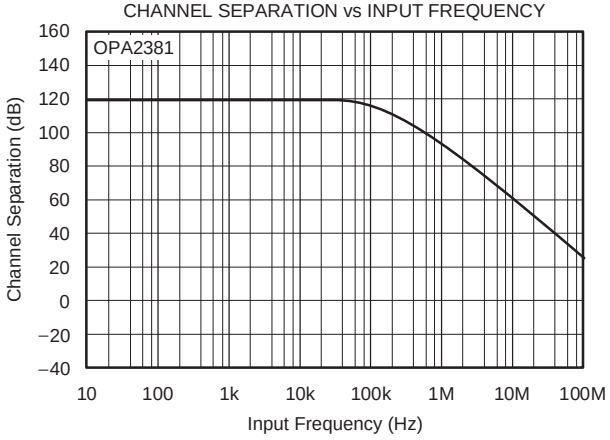
OVERLOAD RECOVERY



INPUT VOLTAGE NOISE SPECTRAL DENSITY



CHANNEL SEPARATION vs INPUT FREQUENCY



APPLICATIONS INFORMATION

BASIC OPERATION

The OPA381 is a high-precision transimpedance amplifier with very low 1/f noise. Due to its unique architecture, the OPA381 has excellent long-term input voltage offset stability.

The OPA381 performance results from an internal auto-zero amplifier combined with a high-speed amplifier. The OPA381 has been designed with circuitry to improve overload recovery and settling time over that achieved by a traditional composite approach. It has been specifically designed and characterized to accommodate circuit options to allow 0V output operation (see Figure 3).

The OPA381 is used in inverting configurations, with the noninverting input used as a fixed biasing point. Figure 1 shows the OPA381 in a typical configuration. Power-supply pins should be bypassed with 1µF ceramic or tantalum capacitors. Electrolytic capacitors are not recommended.

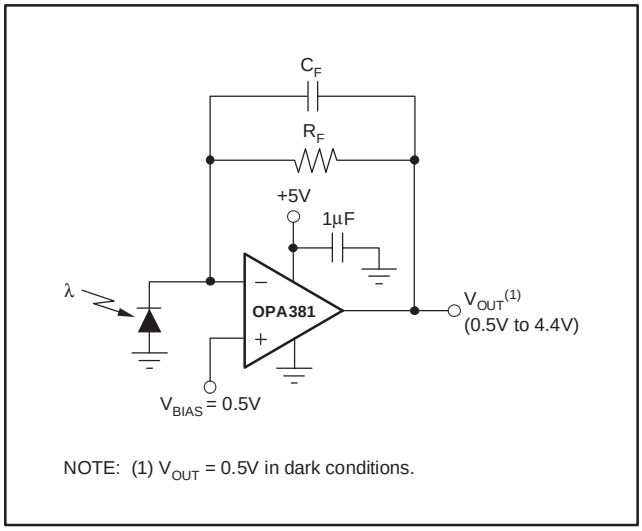


Figure 1. OPA381 Typical Configuration

OPERATING VOLTAGE

OPA381 series op amps are fully specified from 2.7V to 5.5V over a temperature range of −40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics.

INTERNAL OFFSET CORRECTION

The OPA381 series op amps use an auto-zero topology with a time-continuous 18MHz op amp in the signal path. This amplifier is zero-corrected every 100µs using a proprietary technique. Upon power-up, the amplifier requires approximately 400µs to achieve specified V_{OS} accuracy, which includes one full auto-zero cycle of approximately 100µs and the start-up time for the bias circuitry. Prior to this time, the amplifier will function properly but with unspecified offset voltage.

This design has virtually no aliasing and low noise. Zero correction occurs at a 10kHz rate, but there is virtually no fundamental noise energy present at that frequency due to internal filtering. For all practical purposes, any glitches have energy at 20MHz or higher and are easily filtered, if necessary. Most applications are not sensitive to such high-frequency noise, and no filtering is required.

INPUT VOLTAGE

The input common-mode voltage range of the OPA381 series extends from V− to (V+) –1.8V. With input signals above this common-mode range, the amplifier will no longer provide a valid output value, but it will not latch or invert.

INPUT OVERVOLTAGE PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than approximately 500mV. Momentary voltages greater than 500mV beyond the power supply can be tolerated if the current is limited to 10mA. The OPA381 family features no phase inversion when the inputs extend beyond supplies if the input is current limited.

OUTPUT RANGE

The OPA381 is specified to swing within at least 600mV of the positive rail and 50mV of the negative rail with a 10kΩ load while maintaining good linearity. Swing to the negative rail while maintaining linearity can be extended to 0V—see the section, *Achieving Output Swing to Ground*. See the Typical Characteristic curve, *Output Voltage Swing vs Output Current*.

The OPA381 can swing slightly closer than specified to the positive rail; however, linearity will decrease and a high-speed overload recovery clamp limits the amount of positive output voltage swing available—see Figure 2.

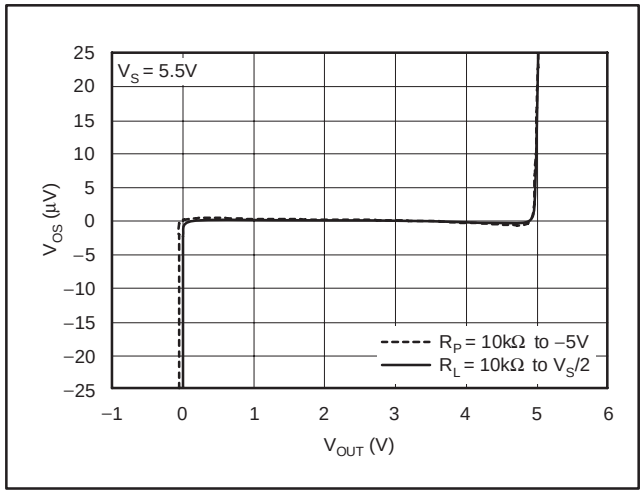


Figure 2. Effect of High-Speed Overload Recovery Clamp on Output Voltage

OVERLOAD RECOVERY

The OPA381 has been designed to prevent output saturation. After being overdriven to the positive rail, it will typically require only 200ns to return to linear operation. The time required for negative overload recovery is greater, *unless* a pulldown resistor connected to a more negative supply is used to extend the output swing all the way to the negative rail—see the following section, *Achieving Output Swing to Ground*.

ACHIEVING OUTPUT SWING TO GROUND

Some applications require output voltage swing from 0V to a positive full-scale voltage (such as +4.096V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach 0V.

The output of the OPA381 can be made to swing to 0V, or slightly below, on a single-supply power source. This extended output swing requires the use of another resistor and an additional negative power supply. A pulldown resistor may be connected between the output and the negative supply to pull the output down to 0V; see Figure 3.

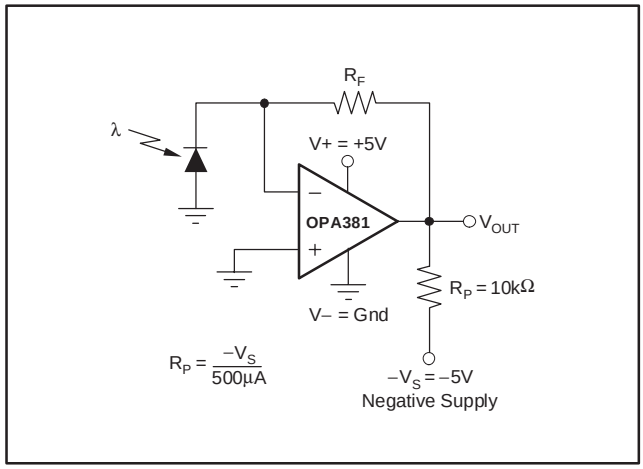
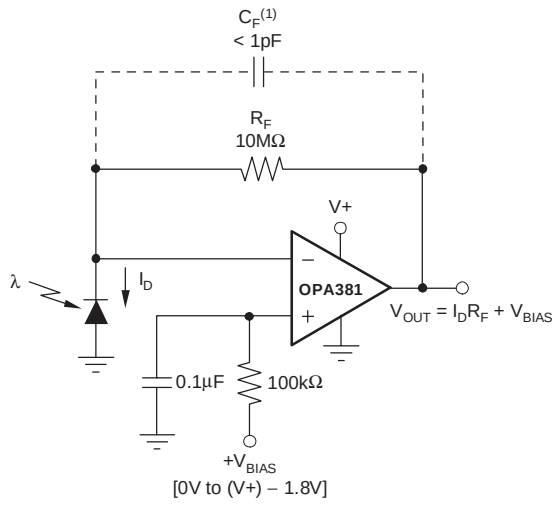


Figure 3. Amplifier with Pull-Down Resistor to Achieve V_{OUT} = 0V

The OPA381 has an output stage that allows the output voltage to be pulled to its negative supply rail using this technique. However, this technique only works with some types of output stages. The OPA381 has been designed to perform well with this method. Accuracy is excellent down to 0V. Reliable operation is assured over the specified temperature range.

BIASING PHOTODIODES IN SINGLE-SUPPLY CIRCUITS

The +IN input can be biased with a positive DC voltage to offset the output voltage and allow the amplifier output to indicate a true *zero* photodiode measurement when the photodiode is not exposed to any light. It will also prevent the added delay that results from coming out of the negative rail. This bias voltage appears across the photodiode, providing a reverse bias for faster operation. An RC filter placed at this bias point will reduce noise. (Refer to Figure 4.) This bias voltage can also serve as an offset bias point for an ADC with range that does not include ground.



NOTE: (1) C_F is optional to prevent gain peaking. It includes the stray capacitance of R_F.

Figure 4. Photodiode with Filtered Reverse Bias Voltage

TRANSIMPEDANCE AMPLIFIER

Wide bandwidth, low input bias current and low input voltage and current noise make the OPA381 an ideal wideband photodiode transimpedance amplifier. Low voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design are shown in Figure 5:

- the total input capacitance (C_{TOT}), consisting of the photodiode capacitance (C_{DIODE}) plus the parasitic common-mode and differential-mode input capacitance (2.5pF + 1pF for the OPA381);
- the desired transimpedance gain (R_F);
- the Gain Bandwidth Product (GBW) for the OPA381 (18MHz).

With these three variables set, the feedback capacitor value (C_F) can be set to control the frequency response. C_{STRAY} is the stray capacitance of R_F, which is 0.2pF for a typical surface-mount resistor.

To achieve a maximally flat 2nd-order Butterworth frequency response, the feedback pole should be set to:

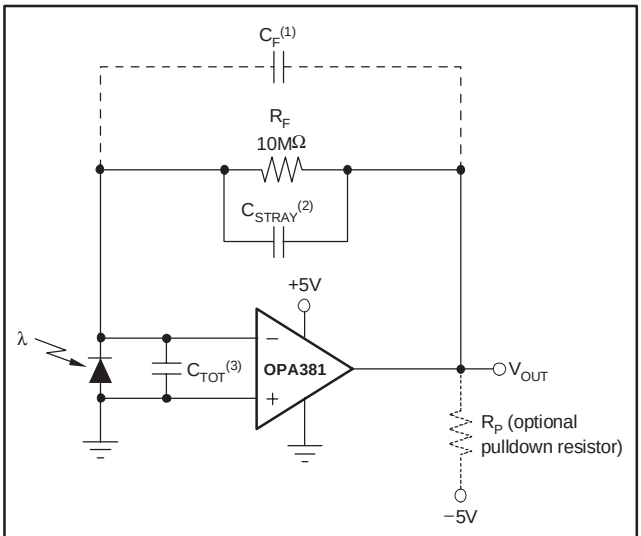
$$\frac{1}{2\pi R_F(C_F + C_{STRAY})} = \sqrt{\frac{GBW}{4\pi R_F C_{TOT}}} \quad (1)$$

Bandwidth is calculated by:

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi R_F C_{TOT}}} Hz \quad (2)$$

These equations will result in maximum transimpedance bandwidth. For even higher transimpedance bandwidth, the high-speed CMOS OPA380 (90MHz GBW), the OPA300 (150MHz GBW), or the OPA656 (230MHz GBW) may be used.

For additional information, refer to Application Bulletin AB−050 (SBOA055), *Compensate Transimpedance Amplifiers Intuitively*, available for download at www.ti.com.



NOTE: (1) C_F is optional to prevent gain peaking.
(2) C_{STRAY} is the stray capacitance of R_F (typically, 0.2pF for a surface-mount resistor).
(3) C_{TOT} is the photodiode capacitance plus OPA381 input capacitance.

Figure 5. Transimpedance Amplifier

TRANSIMPEDANCE BANDWIDTH AND NOISE

Limiting the gain set by R_F can decrease the noise occurring at the output of the transimpedance circuit. However, all required gain should occur in the transimpedance stage, since adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise spectral density produced by R_F increases with the square-root of R_F, whereas the signal increases linearly. Therefore, signal-to-noise ratio is improved when all the required gain is placed in the transimpedance stage.

Total noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor, C_F, across the feedback resistor, R_F, to limit bandwidth (even if not required for stability), if total output noise is a concern.

Figure 6a shows the transimpedance circuit without any feedback capacitor. The resulting transimpedance gain of this circuit is shown in Figure 7. The –3dB point is approximately 3MHz. Adding a 16pF feedback capacitor (Figure 6b) will limit the bandwidth and result in a –3dB point at approximately 200kHz (seen in Figure 7). Output noise will be further reduced by adding a filter (R_{FILTER} and C_{FILTER}) to create a second pole (Figure 6c). This second pole is placed within the feedback loop to maintain the amplifier's low output impedance. (If the pole was placed outside the feedback loop, an additional buffer would be required and would inadvertently increase noise and dc error).

Using R_{DIODE} to represent the equivalent diode resistance, and C_{TOT} for equivalent diode capacitance plus OPA381 input capacitance, the noise zero, f_Z, is calculated by:

$$f_Z = \frac{(R_{DIODE} + R_F)}{2\pi R_{DIODE} R_F (C_{TOT} + C_F)} \quad (3)$$

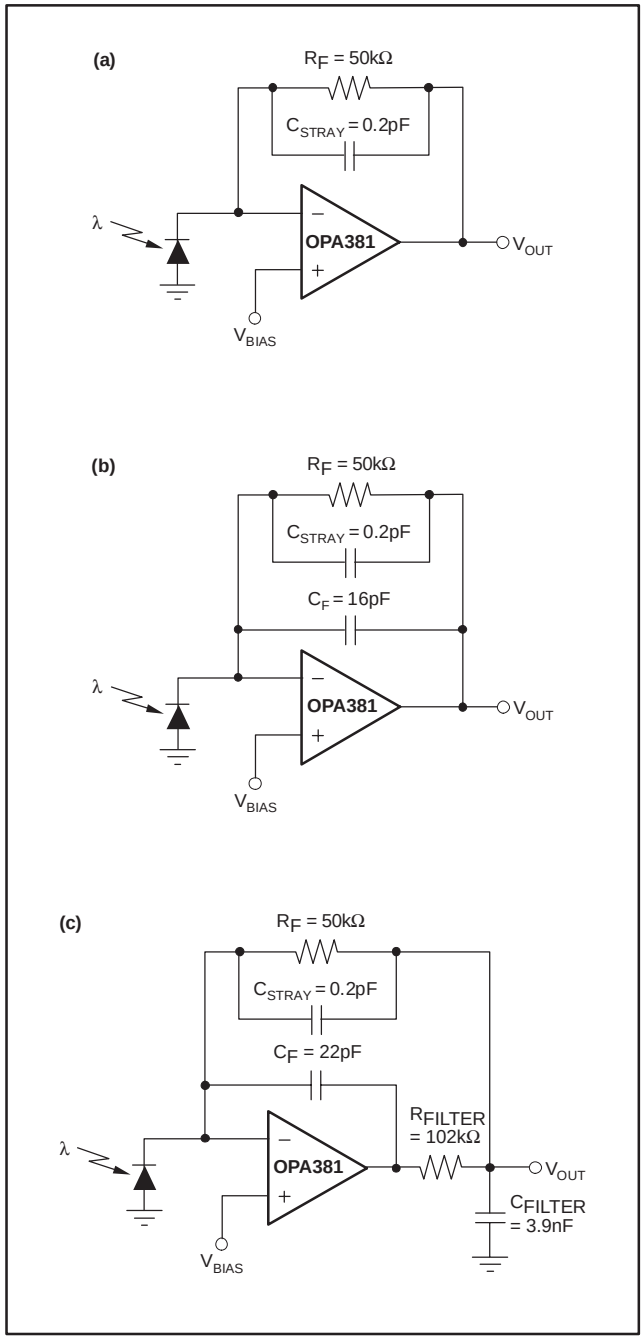


Figure 6. Transimpedance Circuit Configurations with Varying Total and Integrated Noise Gain

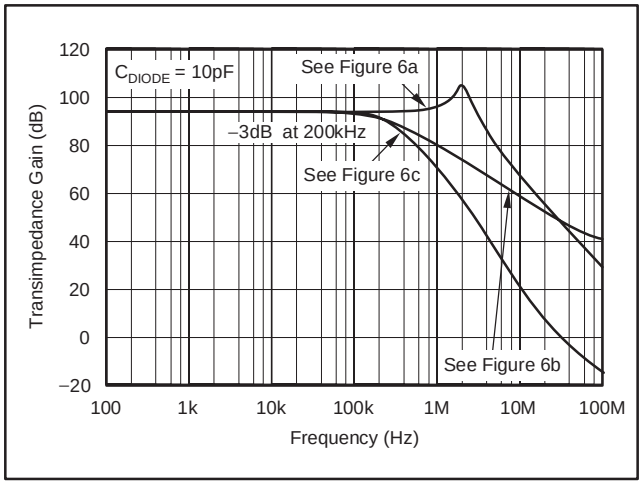


Figure 7. Transimpedance Gains for Circuits in Figure 6

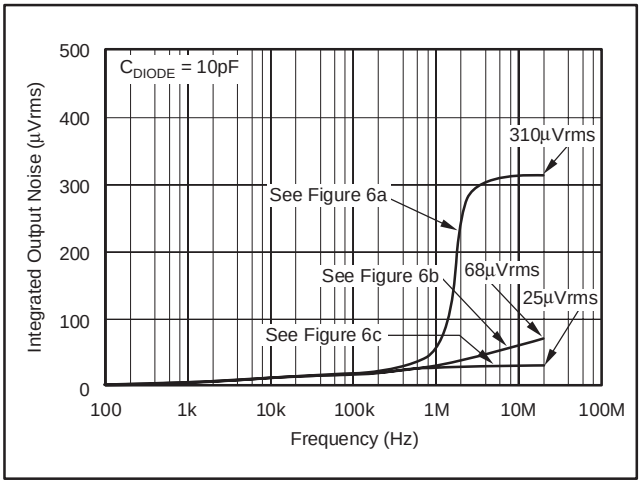


Figure 9. Integrated Output Noise for Circuits in Figure 6

The effects of these circuit configurations on output noise are shown in Figure 8 and on integrated output noise in Figure 9. A 2-pole Butterworth filter (maximally flat in passband) is created by selecting the filter values using the equation:

$$C_F R_F = 2C_{FILTER} R_{FILTER} \quad (4)$$

The circuit in Figure 6b rolls off at 20dB/decade. The circuit with the additional filter shown in Figure 6c rolls off at 40dB/decade, resulting in improved noise performance.

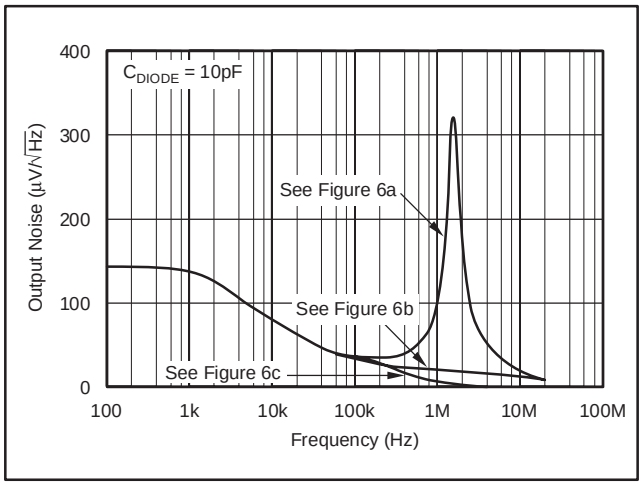


Figure 8. Output Noise for Circuits in Figure 6

Figure 10 shows the effects of diode capacitance on integrated output noise, using the circuit in Figure 6c.

For additional information, refer to *Noise Analysis of FET Transimpedance Amplifiers* (SBOA060), and *Noise Analysis for High Speed Op Amps* (SBOA066), available for download from the TI web site.

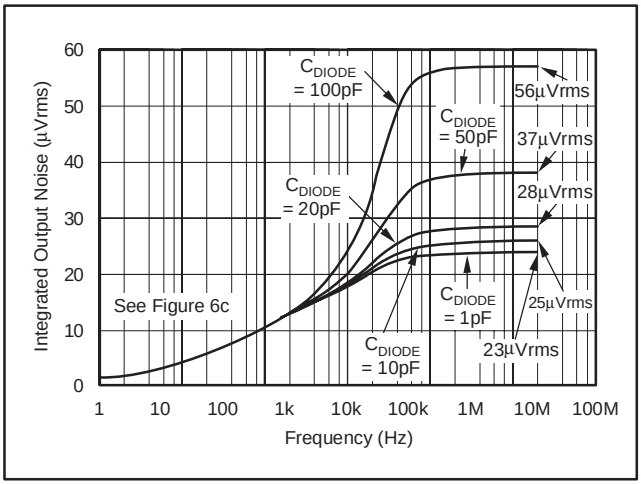


Figure 10. Integrated Output Noise for Various Values of C_{DIODE} for Circuit in Figure 6c

BOARD LAYOUT

Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to be amplified (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce its capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.

Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage. See Figure 11.

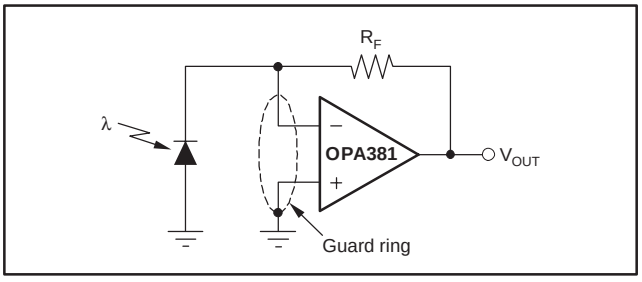


Figure 11. Connection of Input Guard

OTHER WAYS TO MEASURE SMALL CURRENTS

Logarithmic amplifiers are used to compress extremely wide dynamic range input currents to a much narrower range. Wide input dynamic ranges of 8 decades, or 100pA to 10mA, can be accommodated for input to a 12-bit ADC. (Suggested products: LOG101, LOG102, LOG104, LOG112.)

Extremely small currents can be accurately measured by integrating currents on a capacitor. (Suggested product: IVC102.)

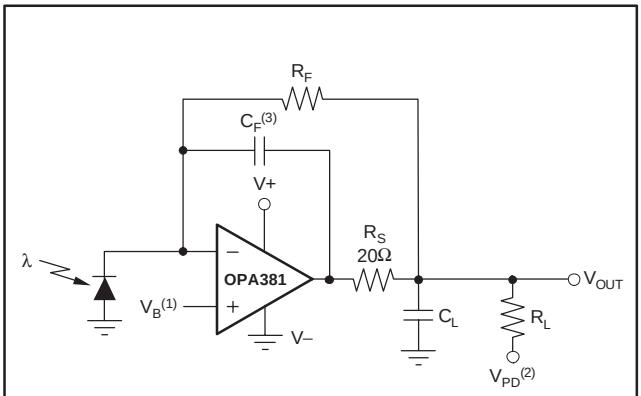
Low-level currents can be converted to high-resolution data words. (Suggested product: DDC112.)

For further information on the range of products available, search www.ti.com using the above specific model names or by using keywords *transimpedance* and *logarithmic*.

CAPACITIVE LOAD AND STABILITY

The OPA381 series op amps can drive greater than 100pF pure capacitive load. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads. See the *Phase Margin vs Load Capacitance* typical characteristic curve.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10Ω to 20Ω resistor inside the feedback loop, as shown in Figure 12. This reduces ringing with large capacitive loads while maintaining DC accuracy.



NOTES: (1) V_B = GND or pedestal voltage to reverse bias the photodiode.
(2) V_{PD} = GND or –5V.
(3) $C_F \times R_F \geq 2C_L \times R_S$.

Figure 12. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive

DRIVING 16-BIT ANALOG-TO-DIGITAL CONVERTERS (ADC)

The OPA381 series is optimized for driving a 16-bit ADC such as the ADS8325. The OPA381 op amp buffers the converter input capacitance and resulting charge injection while providing signal gain. Figure 13 shows the OPA381 in a single-ended method of interfacing the ADS8325 16-bit, 100kSPS ADC. For additional information, refer to the ADS8325 data sheet.

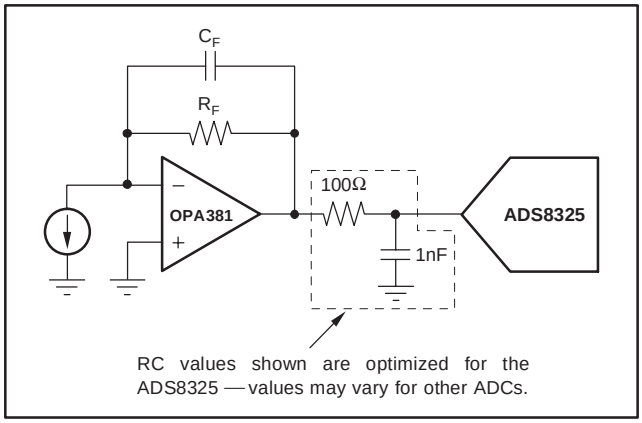


Figure 13. Driving 16-Bit ADCs

INVERTING AMPLIFIER

Its excellent dc precision characteristics make the OPA381 also useful as an inverting amplifier. Figure 14 shows it configured for use on a single-supply set to a gain of 10.

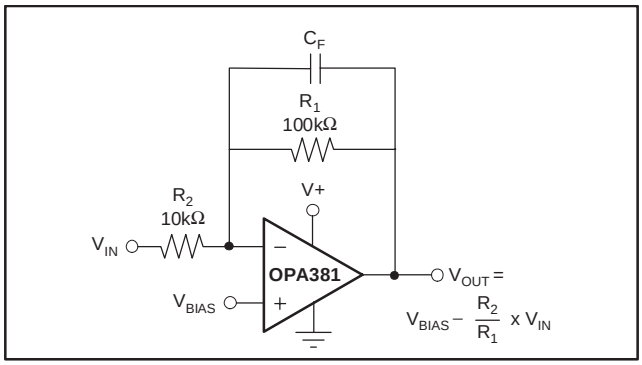


Figure 14. Inverting Gain

PRECISION INTEGRATOR

With its low offset voltage, the OPA381 is well-suited for use as an integrator. Some applications require a means to reset the integration. The circuit shown in Figure 15 uses a mechanical switch as the reset mechanism. The switch is opened at the beginning of the integration period. It is shown in the open position, which is the integration mode. With the values of R_1 and C_1 shown, the output changes −1V/s per volt of input.

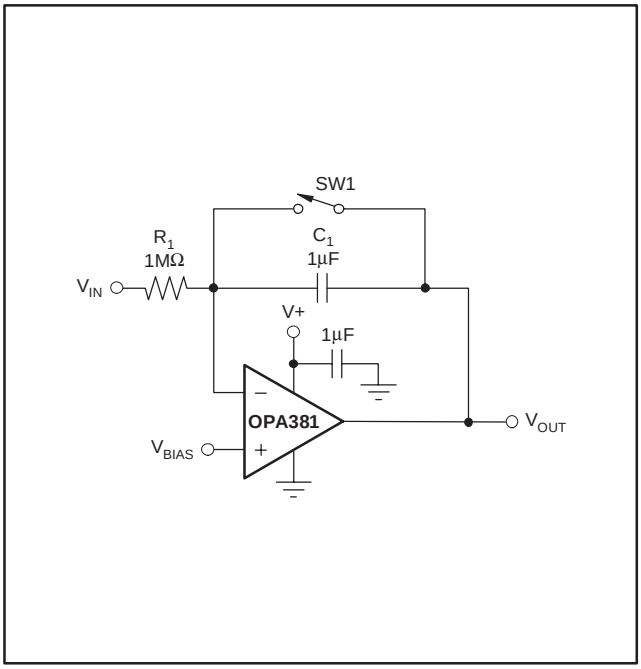


Figure 15. Precision Integrator

DFN (DRB) THERMALLY-ENHANCED PACKAGE

One of the package options for the OPA381 and OPA2381 is the DFN-8 package, a thermally-enhanced package designed to eliminate the use of bulky heat sinks and slugs traditionally used in thermal packages. The absence of external leads eliminates bent-lead concerns and issues.

Although the power dissipation requirements of a given application might not require a heat sink, for mechanical reliability, the exposed power pad must be soldered to the board and connected to V− (pin 4). This package can be easily mounted using standard PCB assembly techniques. See Application Note SLUA271, *QFN/SON PCB Attachment*, located at www.ti.com. These DFN packages have reliable solderability with either SnPb or Pb-free solder paste.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2381AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	-40 to 125	A62
OPA2381AIDGKR.B	Active	Production	null (null) |	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	See OPA2381AIDGKR	A62
OPA2381AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	-40 to 125	A62
OPA2381AIDGKT.B	Active	Production	null (null) |	250 | SMALL T&R	-	Call TI	Level-2-260C-1 YEAR	See OPA2381AIDGKT	A62
OPA2381AIDRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A63
OPA2381AIDRBT.B	Active	Production	null (null) |	250 | SMALL T&R	-	NIPDAU	Level-2-260C-1 YEAR	See OPA2381AIDRBT	A63
OPA381AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	-40 to 125	A64
OPA381AIDGKR.B	Active	Production	null (null) |	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	See OPA381AIDGKR	A64
OPA381AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	-40 to 125	A64
OPA381AIDGKT.B	Active	Production	null (null) |	250 | SMALL T&R	-	Call TI	Level-2-260C-1 YEAR	See OPA381AIDGKT	A64
OPA381AIDRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A65
OPA381AIDRBT.B	Active	Production	null (null) |	250 | SMALL T&R	-	NIPDAU	Level-2-260C-1 YEAR	See OPA381AIDRBT	A65

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

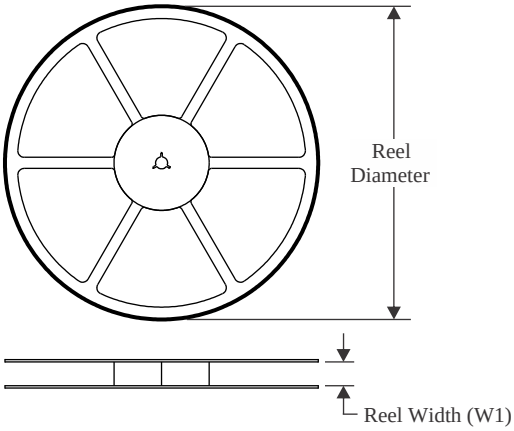
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

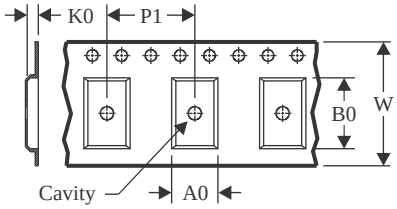
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

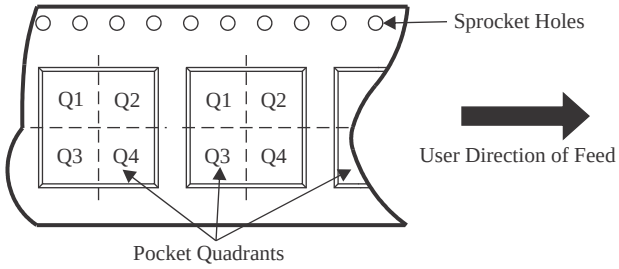


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

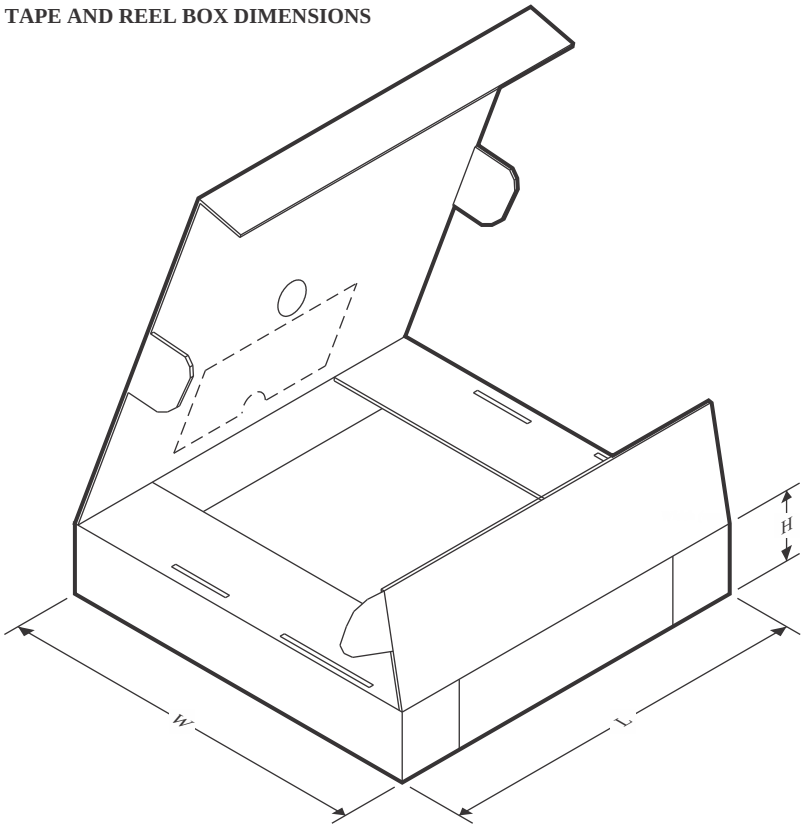
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2381AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA381AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2381AIDRBT	SON	DRB	8	250	210.0	185.0	35.0
OPA381AIDRBT	SON	DRB	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

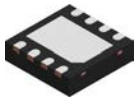
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

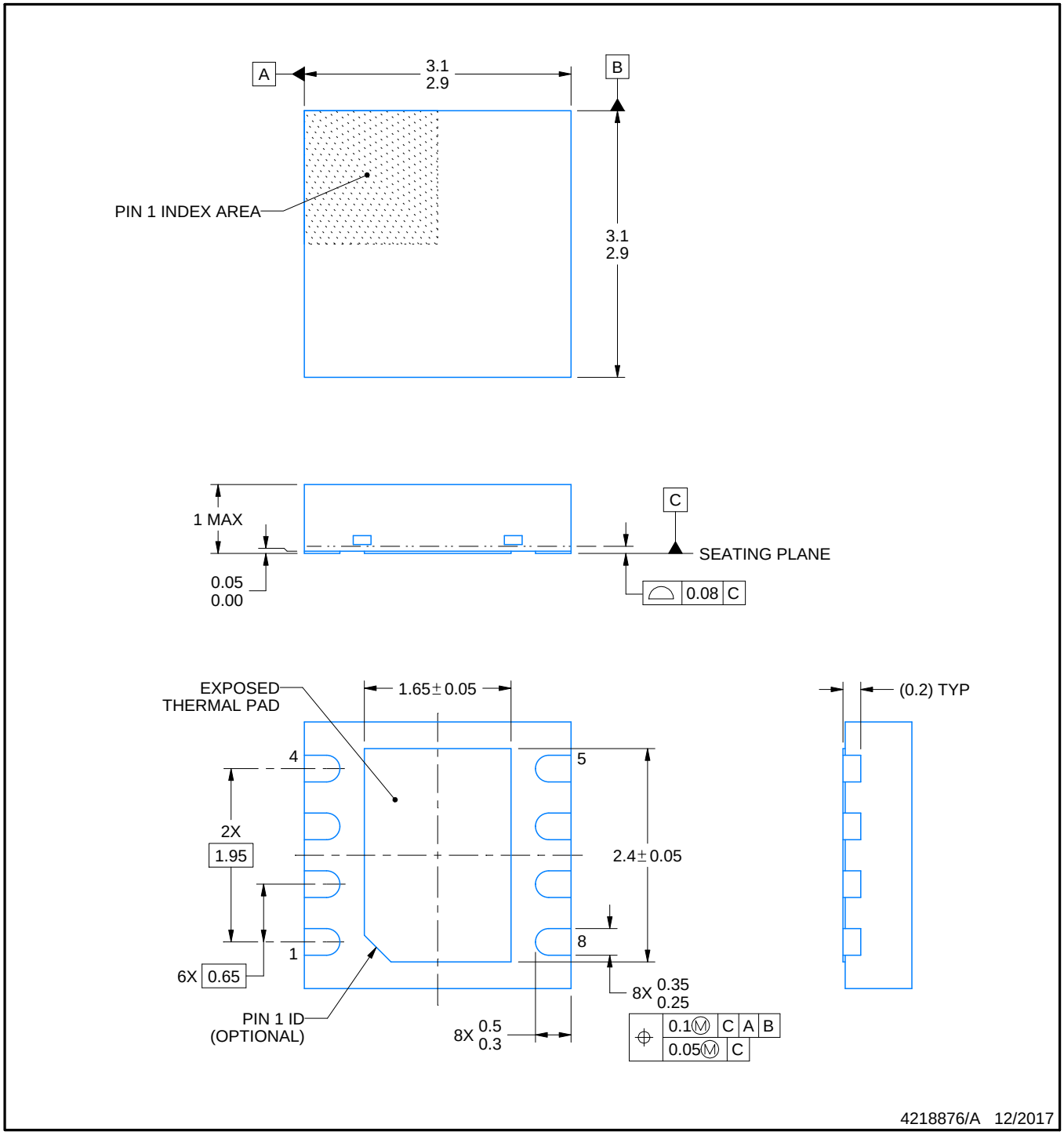
DRB0008B



PACKAGE OUTLINE

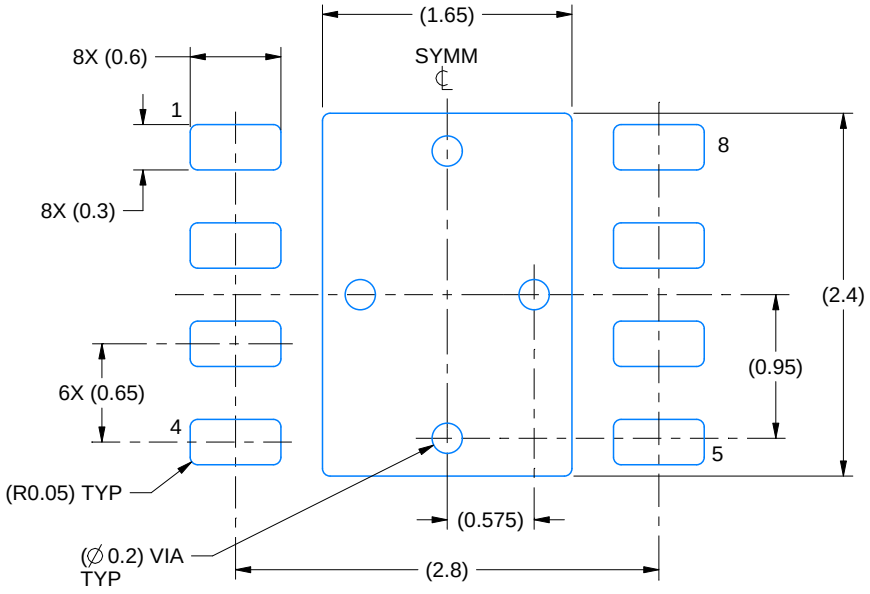
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

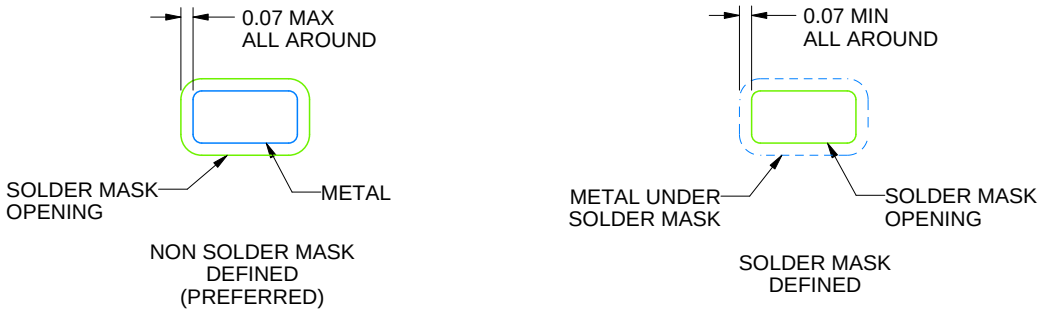


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

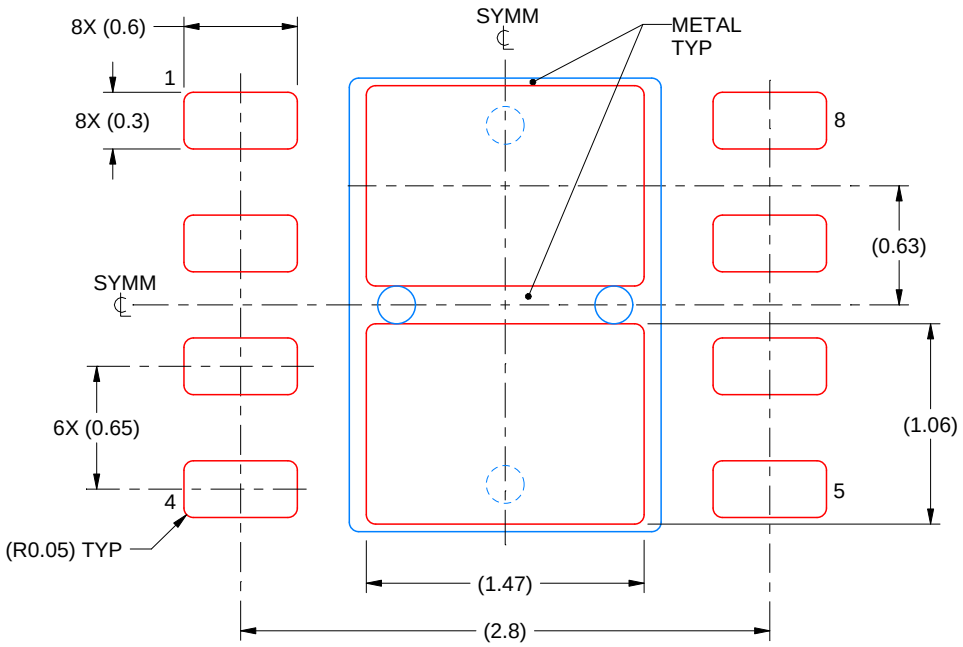


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

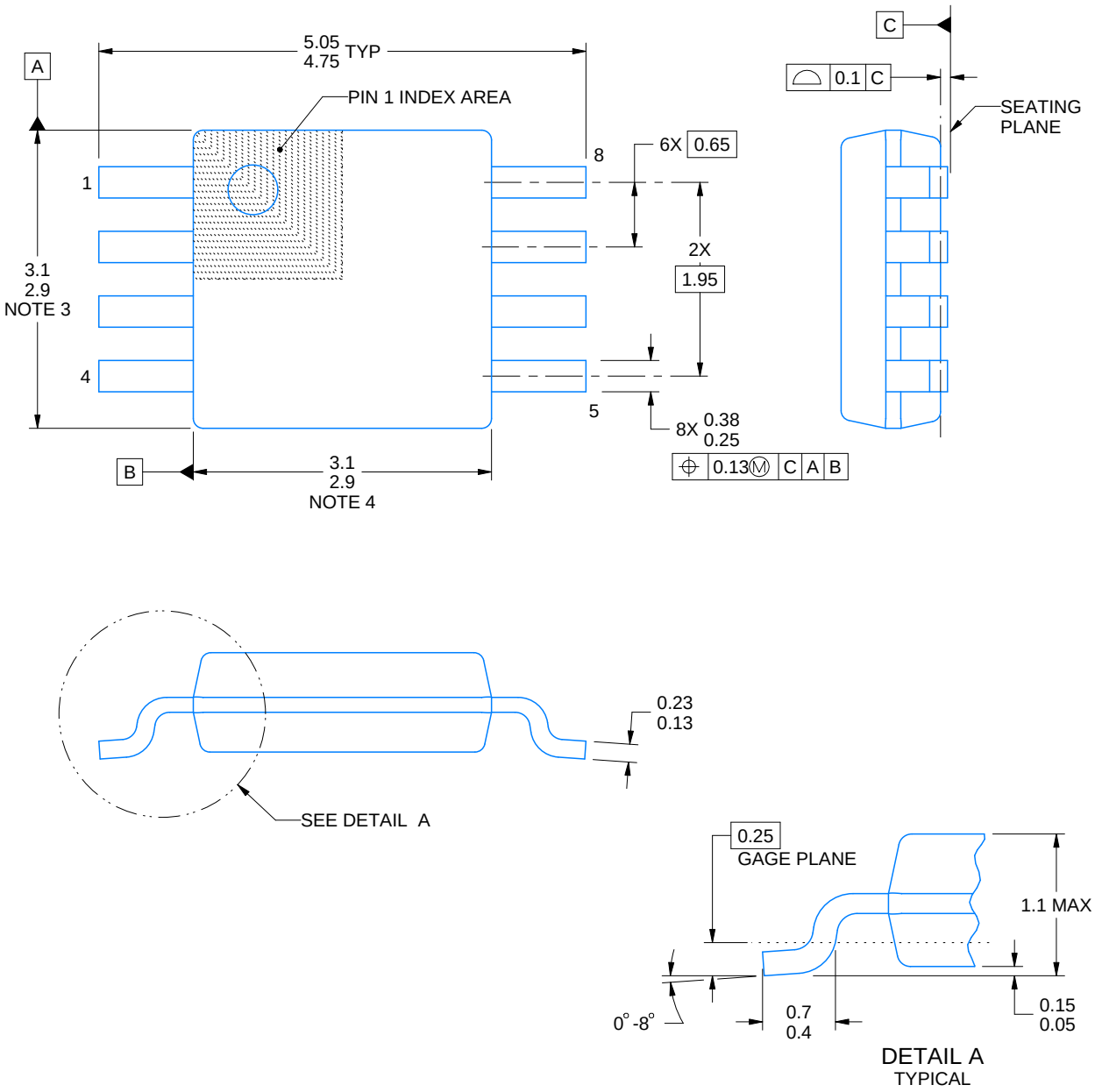
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

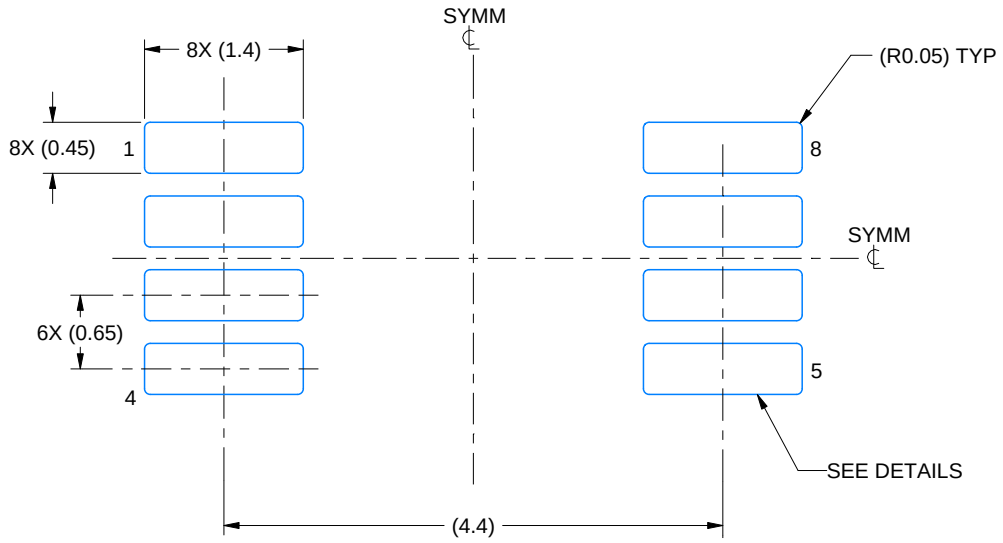
SMALL OUTLINE PACKAGE



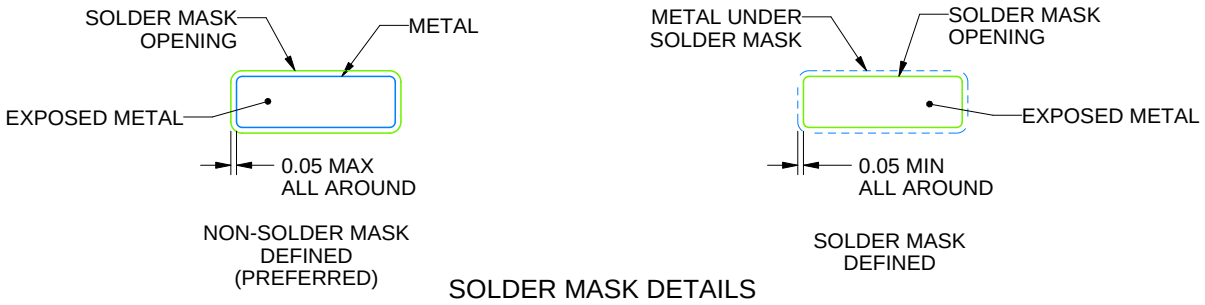
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

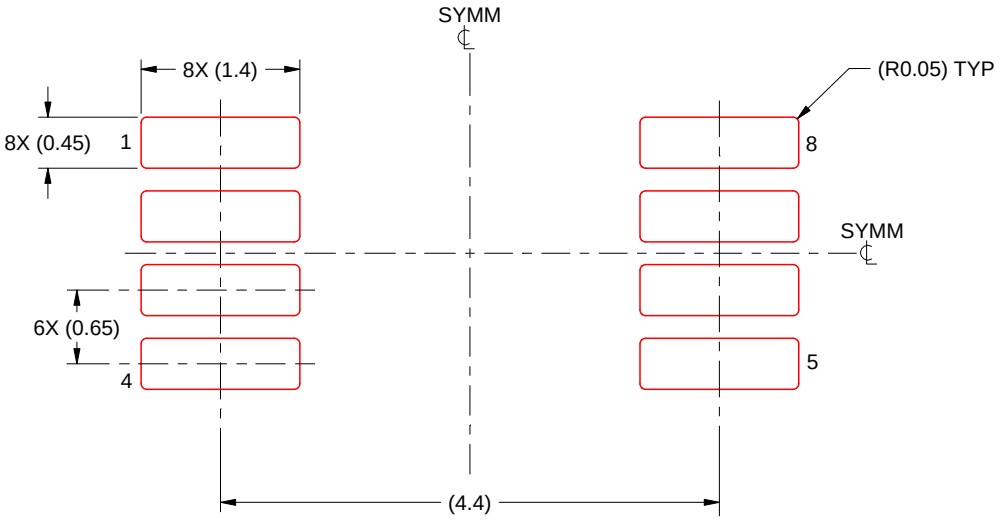


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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