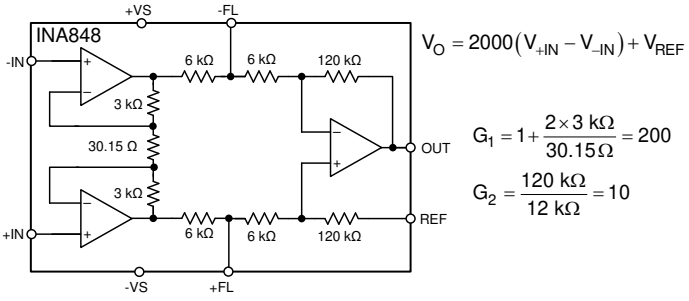
INA848 具有 2000 固定增益的超低噪声 (1.5nV/√Hz)、高带宽仪表放大器

1 特性

- 固定增益为 2000V/V
- 访问内部节点以进行过滤
- 超低噪声：1.5nV/ √Hz 输入电压噪声（最大值）
- 精密超级 ß 输入性能：
  - 低失调电压：35µV（最大值）
  - 低失调电压漂移：0.45 µ V/°C（上限）
  - 低输入偏置电流：25nA（典型值）
  - 低增益漂移：5ppm/°C（最大值）
- 带宽：2.8 MHz
- 压摆率：45 V/µs
- 共模抑制：132dB（最小值）
- 电源电压范围：
  - 单电源：8 V 至 36 V
  - 双电源：±4 V 至 ±18V
- 额定温度范围：
  - –40°C 至 +125°C
- 封装：8 引脚 SOIC

2 应用

- 外科手术设备
- 心电图 (ECG)
- 超声波扫描仪
- 半导体测试
- 数据采集 (DAQ)
- 振动分析



INA848 简化版内部原理图

3 说明

INA848 是一款固定增益仪表放大器，针对高精度测量（例如超小的快速差动输入信号）进行了优化。TI 的超 β 拓扑提供了非常低的输入偏置电流和电流噪声。匹配良好的晶体管有助于实现非常低的失调电压和温漂。匹配内部电阻器可在整个输入电压范围内产生 132dB 的较高共模抑制比，以及超低的增益漂移误差 5ppm/ºC（最大值）。

INA848 的电流反馈拓扑可在固定增益为 2000 的情况下产生 2.8MHz 的宽带宽，从而无需后续增益级。1.3nV/ √Hz 的超低本底噪声更大限度地降低了与高分辨率模数转换器 (ADC) 对接时对等效位数 (ENOB) 的影响。INA848 提供了在增益级（引脚 2 和 3）之间添加滤波器的灵活性，可保持足够的信号完整性。

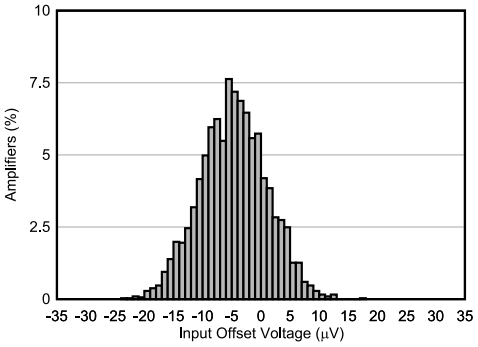
凭借这些独特的特性，INA848 成为要求高精度测量（例如高端医疗仪器、脑电图、振动传感和位移测量）的应用的理想选择。

该器件专为 8V 至 36V 单电源或 ±4V 至 ±18V 双电源而设计。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
INA848	SOIC (8)	4.90mm × 3.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



输入失调电压的典型分布

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

DATE	REVISION	NOTES
September 2020	*	Initial release

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5 Device Comparison Table

DEVICE	DESCRIPTION
INA821	35-μV V_{OS}, 0.4 μV/°C V_{OS} drift, 7-nV/ √ Hz Noise, HighBandwidth, Precision Instrumentation Amplifier
INA819	35-μV V_{OS}, 0.4 μV/°C V_{OS} Drift, 8-nV/ √ Hz Noise, Low-Power, Precision Instrumentation Amplifier
INA333	25-μV V_{OS}, 0.1 μV/°C V_{OS} drift, 1.8-V to 5-V, RRO, 50-μA I_Q, chopper-stabilized INA
PGA280	20-mV to ±10-V programmable gain IA with 3-V or 5-V differential output; analog supply up to ±18 V
PGA112	Precision programmable gain op amp with SPI

6 Pin Configuration and Functions

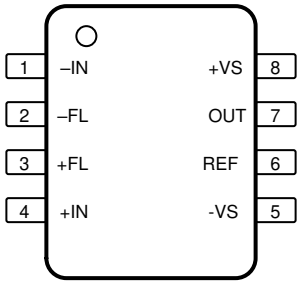


图 6-1. D Package, 8-Pin SOIC, Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	1	I	Negative (inverting) input
+IN	4	I	Positive (noninverting) input
OUT	7	O	Output
–FL	2	I	Negative Filter Terminal.
+FL	3	I	Positive Filter Terminal.
REF	6	I	Reference input. This pin must be driven by a low impedance source.
–VS	5	—	Negative supply
+VS	8	—	Positive supply

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply, V_S = (+V_S)		40	V
		Dual supply, V_S = (+V_S) – (–V_S)		±20	
V_{IN}	Signal input pins	Common Mode (2)	(–V_S) – 0.5	(+V_S) + 0.5	V
		Differential (3)		±0.5	
V_{REF}	VREF pin		(–V_S) – 0.5	(+V_S) + 0.5	V
V_{FL}	Filter input pins +FL, –FL		(–V_S) – 0.5	(+V_S) + 0.5	V
V_O	Signal output pins maximum voltage		(–V_S) – 0.5	(+V_S) + 0.5	V
I_O	Signal output pins maximum current		–50	50	mA
I_S	Output short-circuit(4)		–50	50	mA
T_A	Operating temperature (5)			125	°C
T_J	Junction temperature (5)			175	°C
T_{stg}	Storage temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that swing more than 0.5 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Input terminals are anti-parallel diode-clamped to each other. Input signals that cause differential voltages of swing more than ± 0.5 V must be current-limited to 10 mA or less.
(4) Short-circuit to V_S / 2.
(5) As a result of the quiescent current, a supply voltage and load-dependent self-heating of the device must be considered.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply, V_S = (+V_S)	8	36	V
		Dual supply, V_S = (+V_S) – (–V_S)	±4	±18	
T_A	Specified temperature		–40	125	°C

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7.4 Thermal Information

THERMAL METRIC(1)		INA848 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, G = 2000 (fixed) and V_{REF} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{OSI}	Input offset voltage			±10	±35	µV
		T_A = –40°C to +125°C(1)			±80	
	Input offset voltage drift	T_A = –40°C to +125°C		±0.1	±0.45	µV/°C
PSRR	Power-supply rejection ratio	±4 V ≤ (V_S) ≤ ±18 V	125	150		dB
Z_{in}	Input impedance			1 || 7		GΩ || pF
	RFI filter, –3-dB frequency			250		MHz
V_{CM}	Operating input voltage(3)	V_S = ±4 V to ±18 V	(–V_S) + 2.5		(+V_S) – 2.5	V
		V_S = ±4 V to ±18 V, T_A = –40°C to +125°C		See 图 7-9		
CMRR	Common-mode rejection ratio	At dc to 60 Hz, RTI (–V_S) + 2.5 V < V_{CM} < (+V_S) – 2.5 V	132	150		dB
		At 50 kHz, RTI (–V_S) + 2.5 V < V_{CM} < (+V_S) – 2.5 V		110		
BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2		25	50	nA
	Input bias current dift	T_A = –40°C to +125°C		40		pA/℃
I_{OS}	Input offset current	V_{CM} = V_S / 2		2	10	nA
	Input offset current drift	T_A = –40°C to +125°C		10		pA/℃
NOISE VOLTAGE						
e_{NI}	Input voltage noise	f = 1 kHz, R_S = 0 Ω		1.3	1.5(2)	nV/√Hz
		f_B = 0.1 Hz to 10 Hz, R_S = 0 Ω		55		nV_{PP}
I_n	Input current noise	f = 1 kHz		1.85		pA/√Hz
		f_B = 0.1 Hz to 10 Hz		75		pA_{PP}
GAIN						
G	First stage gain			200		V/V
	Subtractor stage gain			10		V/V
GE	Total gain error	V_O = ±10 V		0.05	0.15(1) (2)	%
	Total gain drift	T_A = –40°C to +125°C			5(1) (2)	ppm/°C

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7.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, G = 2000 (fixed) and V_{REF} = 0 V (unless otherwise noted)

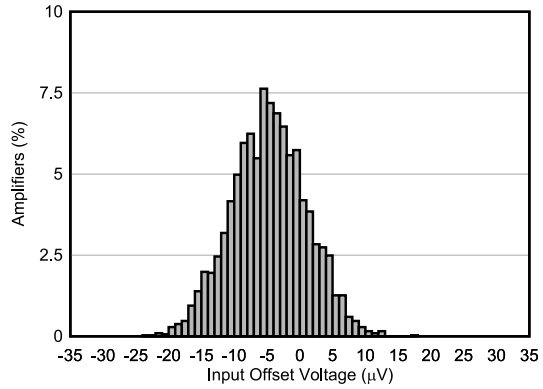
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Total gain nonlinearity	V_O = –10 V to +10 V, no load		10		ppm
THD+N	Total harmonic distortion and noise	f = 20 kHz, V_O = 10 V_{pp}		–109		dBc
HD2	Second-order harmonic distortion	f = 20 kHz, V_O = 10 V_{pp}		–112		dBc
HD3	Third-order harmonic distortion	f = 20 kHz, V_O = 10 V_{pp}		–119		dBc
THD+N	Total harmonic distortion and noise	R_L = 1 MΩ, f = 20 kHz, V_O = 10 V_{pp}		–111		dBc
HD2	Second-order harmonic distortion	R_L = 1 MΩ, f = 20 kHz, V_O = 10 V_{pp}		–117		dBc
HD3	Third-order harmonic distortion	R_L = 1 MΩ, f = 20 kHz, V_O = 10 V_{pp}		–118		dBc
OUTPUT						
	Output voltage swing		(–V_S) + 0.15		(+V_S) – 0.15	V
C_L	Load capacitance	In stable condition		1000		pF
I_{SC}	Short-circuit current	Continuous to V_S / 2		±30		mA
FREQUENCY RESPONSE						
BW	Bandwidth, –3 dB			2.8		MHz
SR	Slew rate	V_{STEP} = 10 V	35[1]	45		V/µs
t_S	Settling time	0.01%, V_{STEP} = 10 V		0.5		µs
		0.001%, V_{STEP} = 10 V		0.9		
REFERENCE INPUT						
R_{IN}	Input impedance			132		kΩ
I_{IN}	Input current			6.5		µA
	Reference input voltage		–V_S		+V_S	V
	Gain to output			1		V/V
	Reference gain error			0.01		%
FILTER INPUTS						
R_{FIL}	Input impedance, filter terminal			6		kΩ
	Voltage range, filter terminal		–V_S		+V_S	V
POWER SUPPLY						
I_Q	Quiescent current	V_{IN} = 0 V		6.2	6.6	mA
		T_A = –40°C to +85°C			7.9	
		T_A = –40°C to +125°C			8.8	

(1) Specified by characterization.
(2) Specified by design.
(3) The input voltage range depends on the common-mode voltage, differential voltage, gain, and reference voltage.

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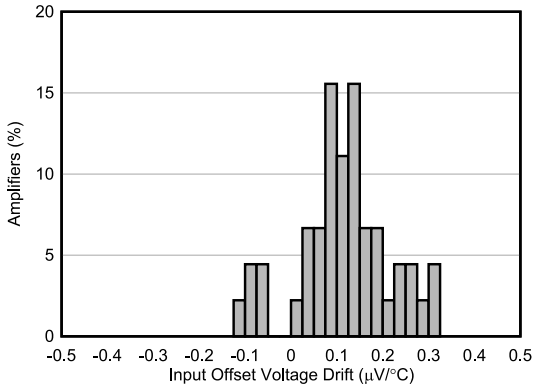
7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 2000 (unless otherwise noted)



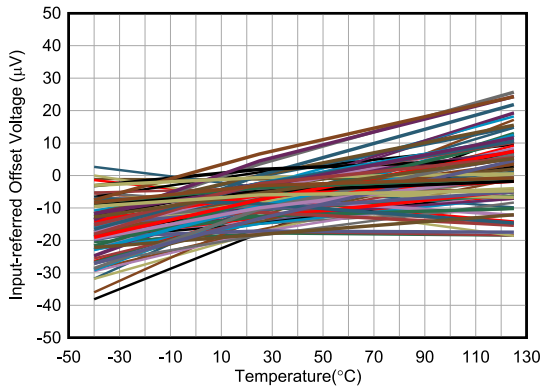
N = 3172, mean = –4.678 µV, std dev = 5.715 µV

图 7-1. Typical Distribution of Input Offset Voltage



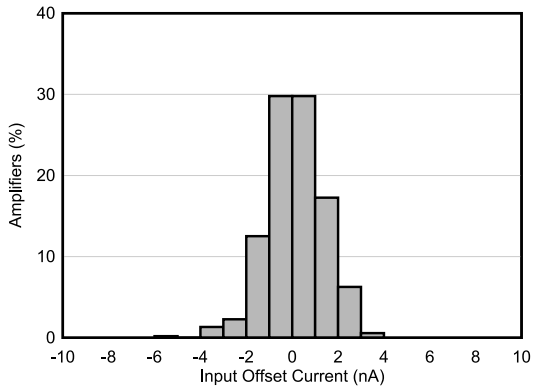
N = 45, mean = 0.116 µV/°C, std dev = 0.102 µV/°C

图 7-2. Typical Distribution of Input Offset Voltage Drift



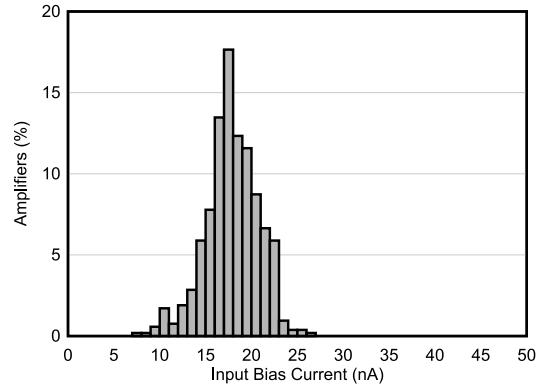
N = 48

图 7-3. Input-referred Offset Voltage vs Temperature



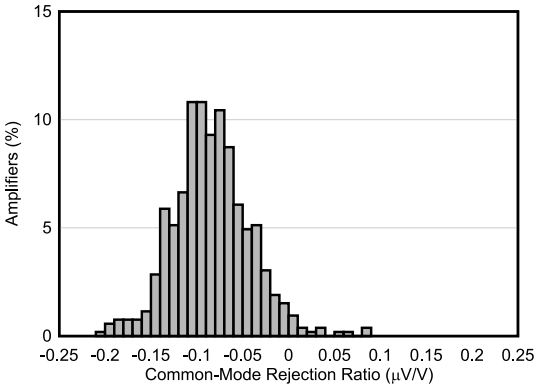
N = 527, mean = 0.1369 nA, std dev = 1.222 nA

图 7-4. Typical Distribution of Input Offset Current



N = 527, mean = 17.876 nA, std dev = 2.875 nA

图 7-5. Typical Distribution of Input Bias Current



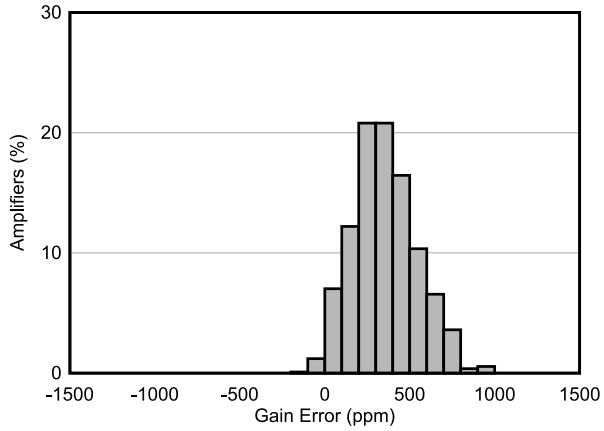
N = 527, mean = -0.0840 µV/V, std dev = 0.0420 µV/V

图 7-6. Typical CMRR Distribution

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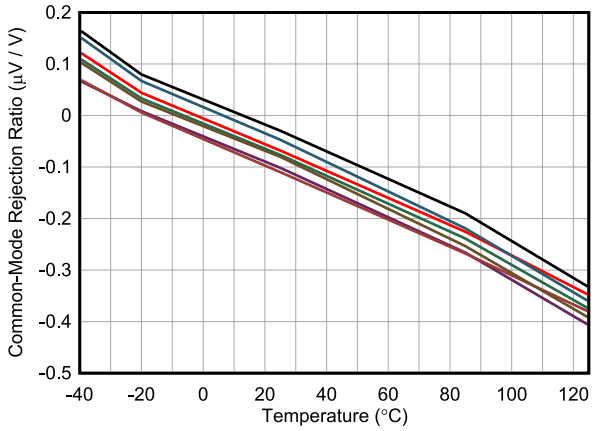
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 2000 (unless otherwise noted)



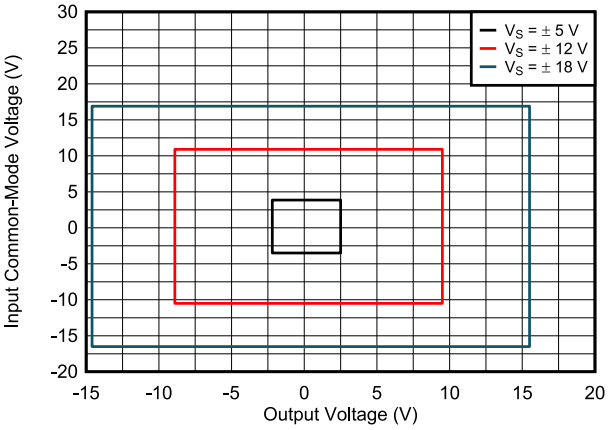
N = 1080, mean = 356.396 ppm, std dev = 186.085 ppm

图 7-7. Typical Distribution of Gain Error



N = 7

图 7-8. CMRR vs Temperature



VREF = 0 V

图 7-9. Input Common-Mode Voltage vs Output Voltage

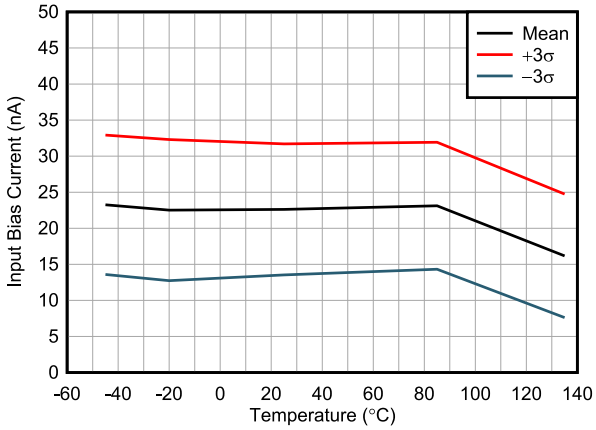


图 7-10. Input Bias Current vs Temperature

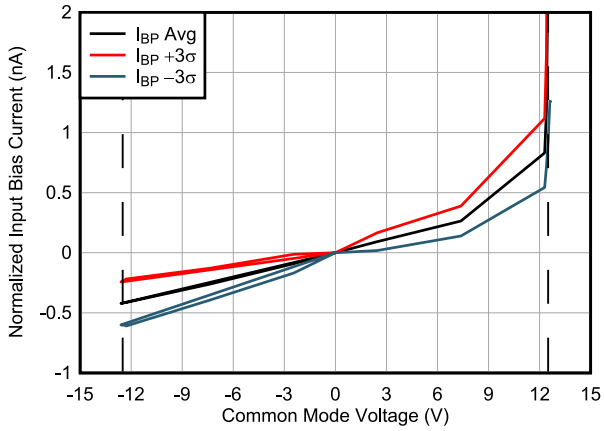


图 7-11. Positive Input Bias Current vs Input Common-Mode Voltage

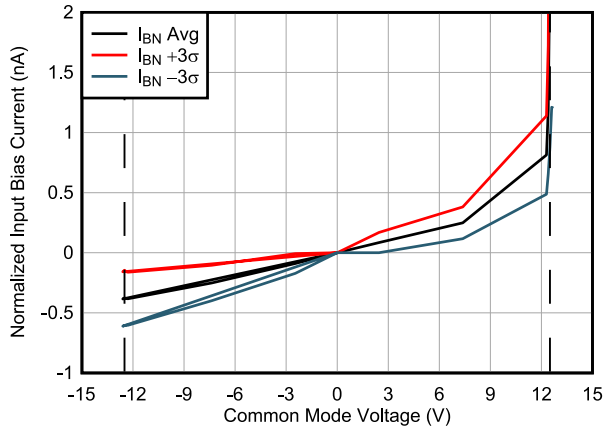


图 7-12. Negative Input Bias Current vs Input Common-Mode Voltage

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7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 2000 (unless otherwise noted)

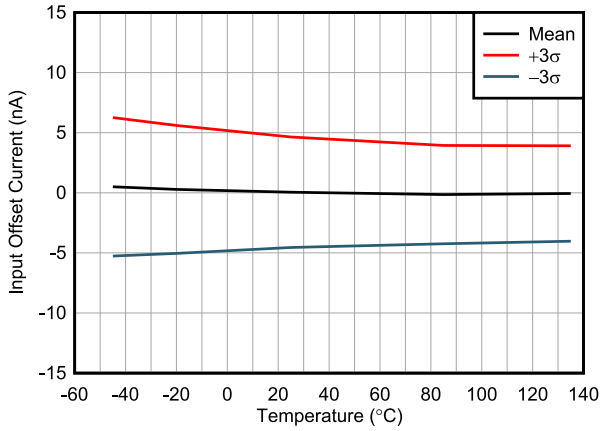


图 7-13. Input Offset Current vs Temperature

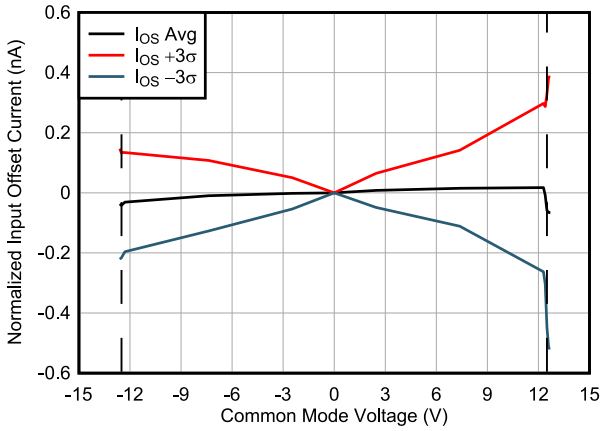


图 7-14. Input Offset Current vs Input Common-Mode Voltage

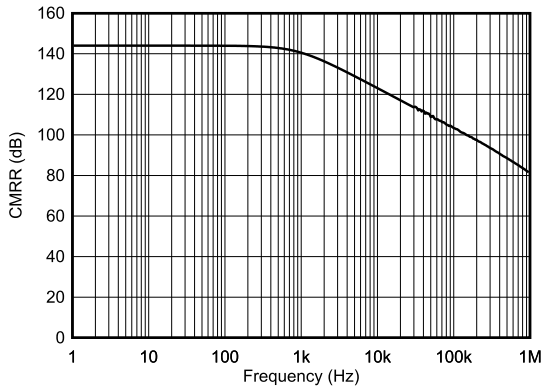


图 7-15. CMRR vs Frequency (RTI)

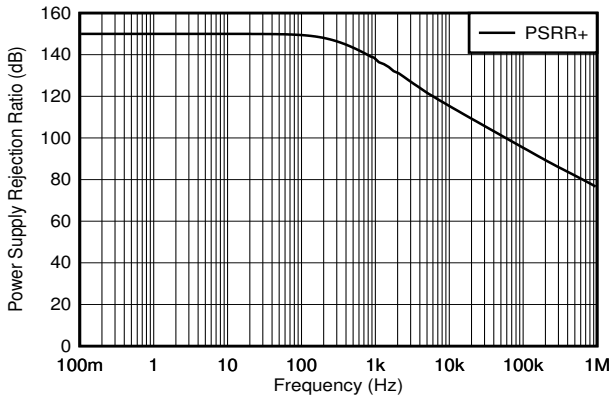


图 7-16. Positive PSRR vs Frequency (RTI)

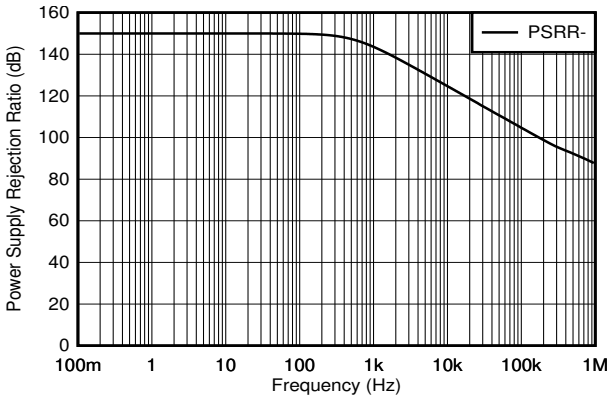


图 7-17. Negative PSRR vs Frequency (RTI)

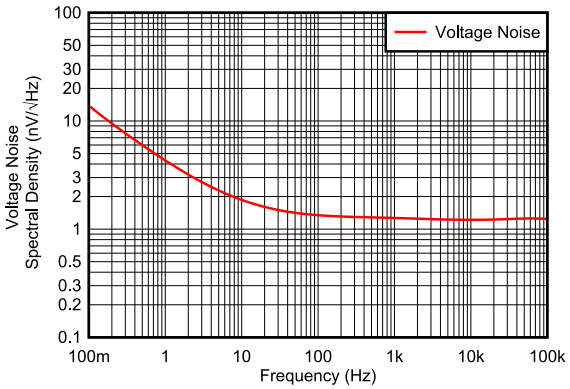


图 7-18. Voltage Noise Spectral Density vs Frequency (RTI)

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7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 2000 (unless otherwise noted)

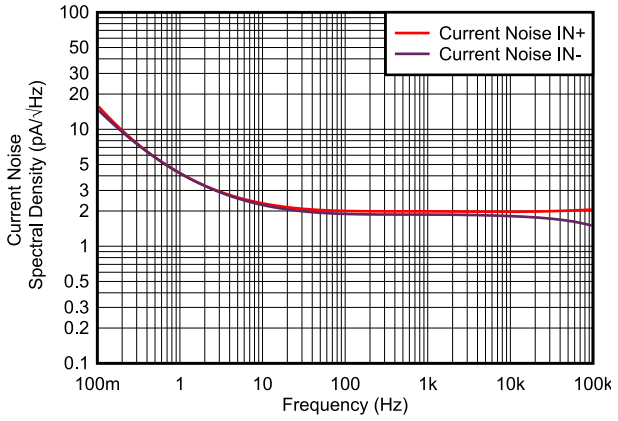


图 7-19. Current Noise Spectral Density vs Frequency (RTI)

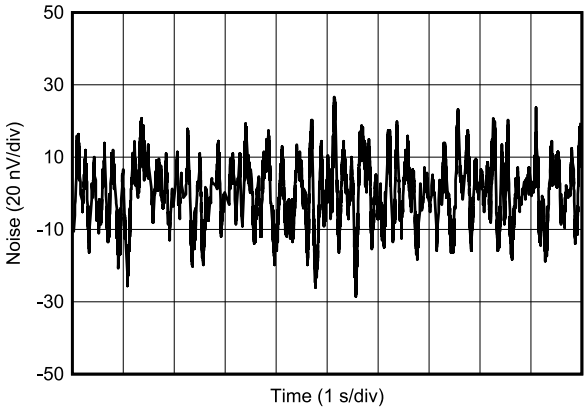


图 7-20. 0.1-Hz to 10-Hz RTI Voltage Noise

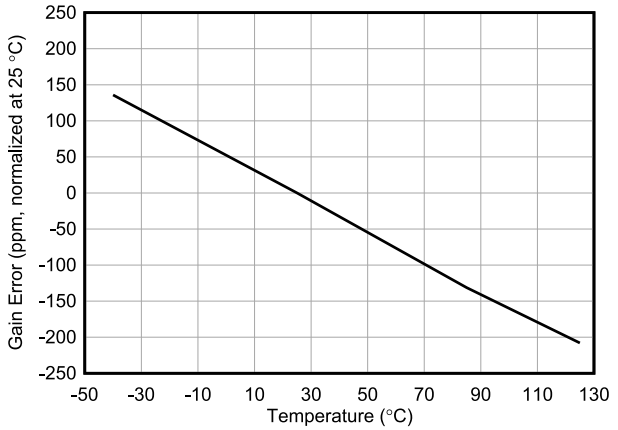


图 7-21. Gain Error vs Temperature

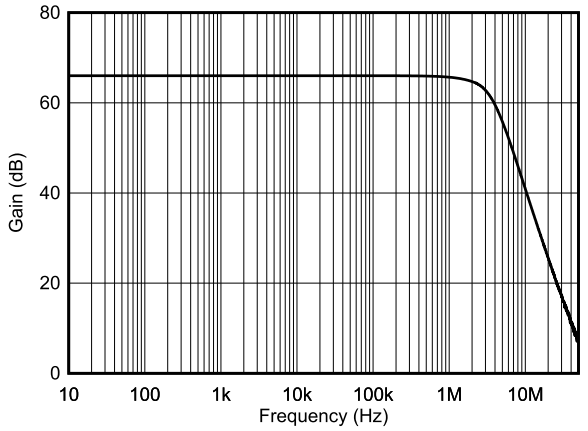


图 7-22. Closed Loop Gain vs Frequency

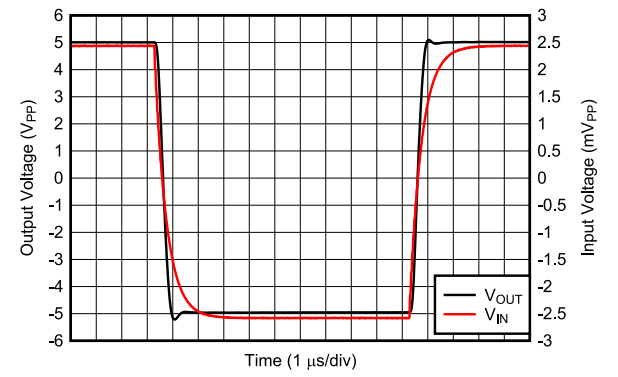


图 7-23. Large-Signal Step Response

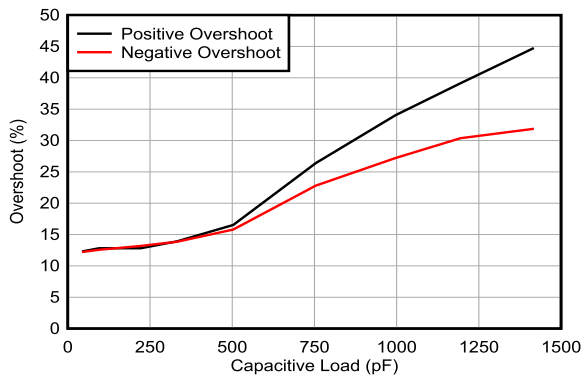


图 7-24. Small Signal Response vs Capacitive Loads

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7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 2000 (unless otherwise noted)

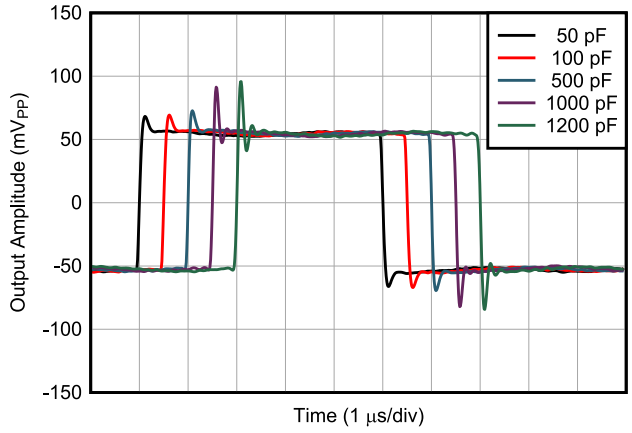


图 7-25. Small Signal Response

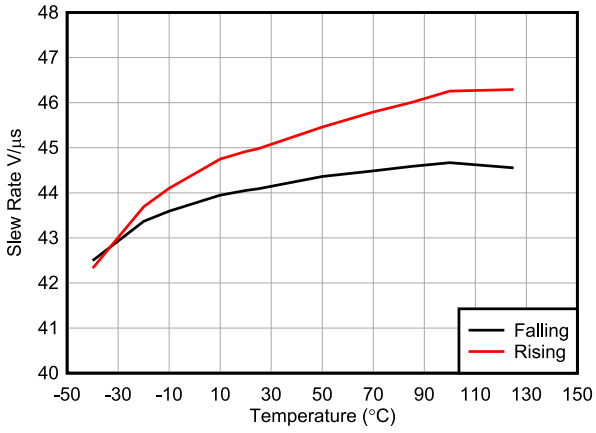


图 7-26. Slew Rate vs Temperature

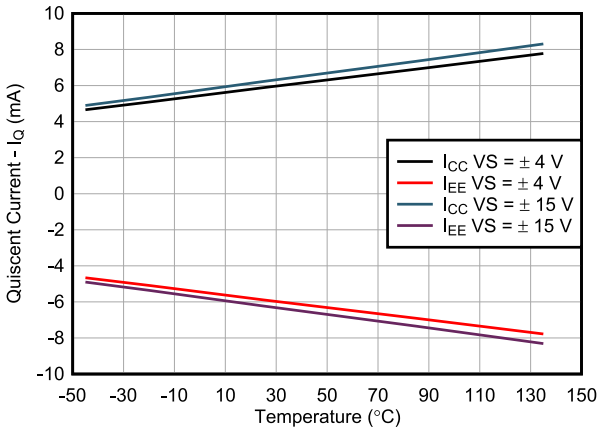


图 7-27. Supply Current vs Temperature

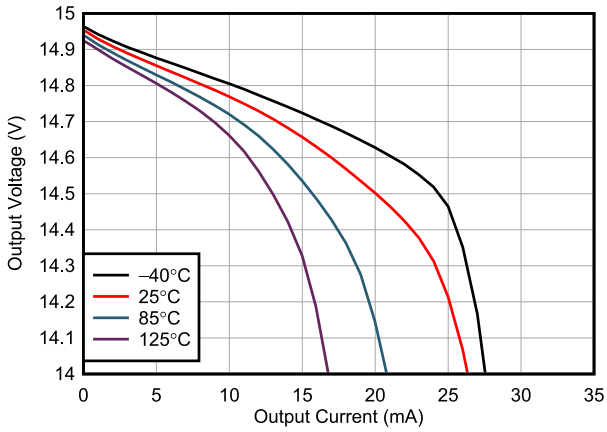


图 7-28. Positive Output Voltage Swing vs Output Current

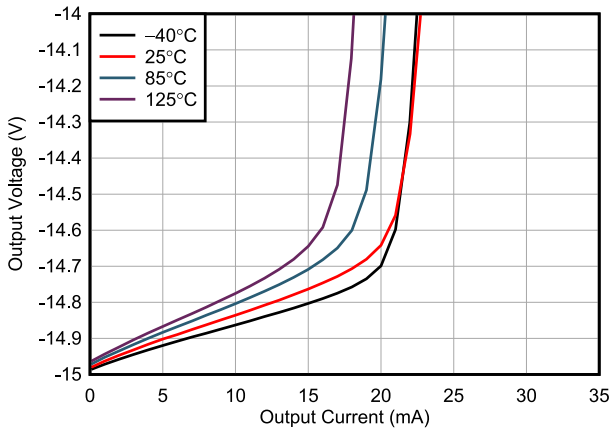


图 7-29. Negative Output Voltage Swing vs Output Current

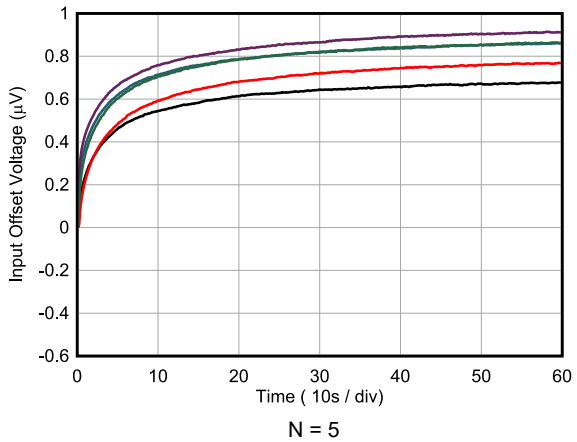


图 7-30. Input-Referred Offset Voltage vs Settling Time

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7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 2000 (unless otherwise noted)

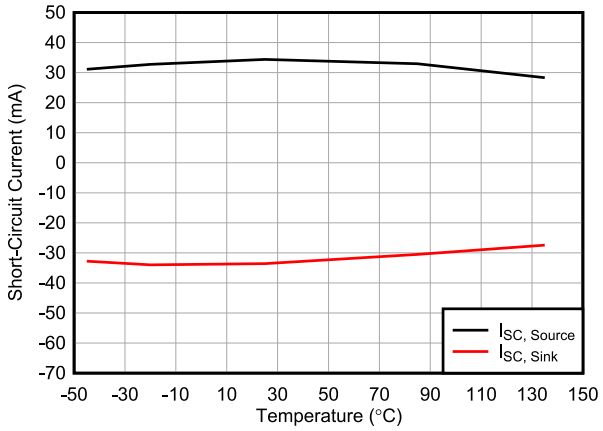


图 7-31. Short Circuit Current (Source + Sink) vs Temperature

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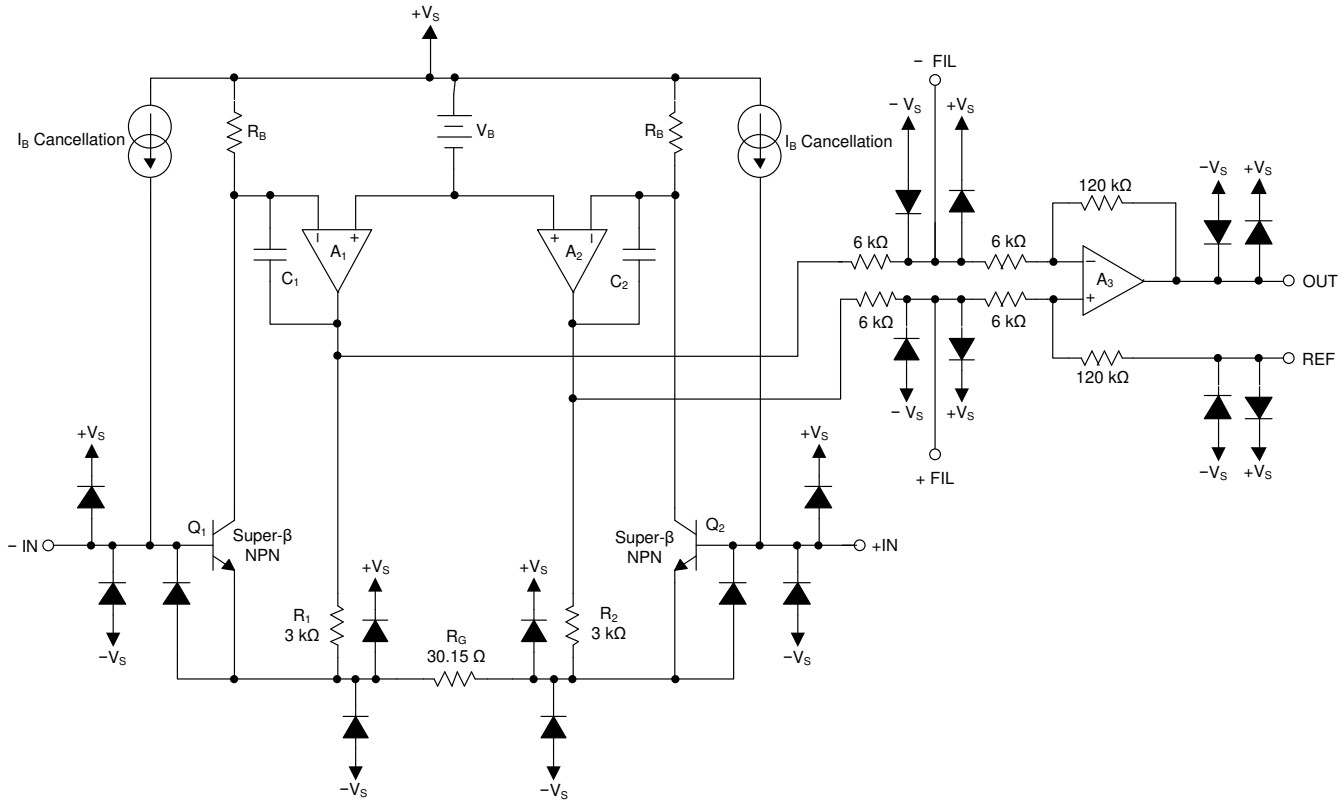
8 Detailed Description

8.1 Overview

The INA848 is a monolithic precision instrumentation amplifier incorporating a current-feedback input stage and a four-resistor difference amplifier output stage. The differential input voltage is buffered by Q_1 and Q_2 and is forced across R_G, which causes a signal current to flow through R_G, R_1, and R_2. The output difference amplifier (A_3) removes the common-mode component of the input signal and refers the output signal to the REF pin. The V_{BE} and voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 0.8 V lower than the input voltages.

In common instrumentation amplifiers, an external gain resistor is used to set the gain. However, this external gain resistor affects the gain drift due to the mismatch in tempertature coefficient between the external and internal resistors. The INA848 integrates the gain setting resistor with a fixed gain of 2000, thus matching the temperature drifts of the resistor network. This integration results in an total gain accuracy of 5 ppm/°C (maximum).

8.2 Functional Block Diagram



8.3 Feature Description

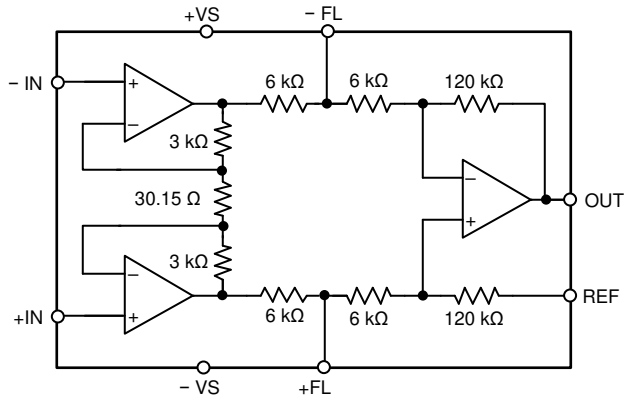
8.3.1 Topology

The INA848 is designed with TI's modern bipolar process that features super-beta input transistors.

Traditional bipolar transistors feature excellent voltage noise and offset drift, but suffer a tradeoff in high input bias current and high input bias current noise.

TI`s super-beta transistors offer the benefits of low voltage noise, low offset voltage drift with an additional improvement in reduction of the input bias current noise.

As shown in 图 8-1, the INA848 is designed with a current feedback input stage that is optimized for high bandwidth in high gains. The device consists of three operational amplifiers configured at the front with a gain stage that integrates the gain resistor. This input stage preamplifies the differential input signal at a gain of 200. The output stage with the difference amplifier provides additional amplification of a gain of 10.



$$V_O = 2000\left(V_{+IN} - V_{-IN}\right) + V_{REF}$$

$$G_1 = 1 + \frac{2 \times 3\ k\Omega}{30.15\ \Omega} = 200$$

$$G_2 = \frac{120\ k\Omega}{12\ k\Omega} = 10$$

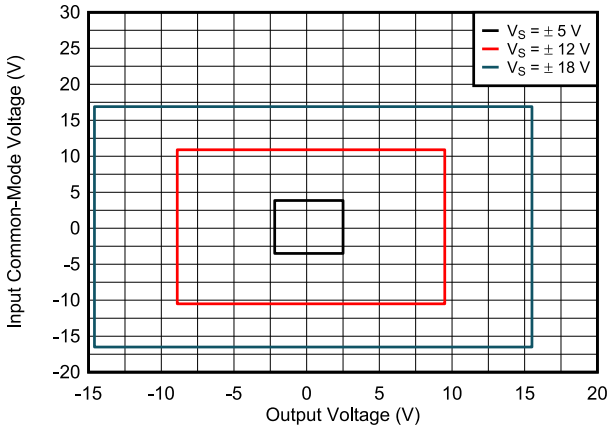
图 8-1. Simplified Diagram of the INA848 With Gain and Output Equations

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8.3.2 Input Common-Mode Range

The typical three-op-amp topology gains up the input differential signal in the front stage and rejects the common-mode signals in the back end at the difference amplifier stage. The difficulty in particular is to excel driving high gains, and thus tiny input signals, and still be able to reject high common-mode signals. A low-noise instrumentation amplifier such as the INA848 is designed for such requirementsh, with the ability to measure the smallest input signals surrounded by noisy or large common-mode voltages.

The methodology here is achieved by splitting up the gain stages. The front end preamplifies the input signal at a gain of 200, and the difference amplifier further amplifiers at a gain of 10. The resulting advantage is that the common-mode range versus the differential signal is improved compared to single gain stage approach, as shown in 图 8-2.



V_S = ± 5 V, ± 12 V, ± 18 V, VREF = 0 V

图 8-2. Input Common-Mode Voltage vs Output Voltage

The INA848 gives the super-beta input stage features very low input bias current as compared to standard bipolar technology. The low input bias current and current noise make the INA848 an excellent choice for high-performance applications. See 图 7-10 through 图 7-12 for reference.

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8.3.3 Input Protection

The inputs of the INA848 device are individually protected for voltages up to ±20 V which is stated in 节 7.1. If these rating cannot be met, additional protection circuitry must be considered at the input pins to minimize the current flowing in case of fault.

During an input overvoltage condition, current flows through the input protection diodes into the power supplies; see 图 8-3 . If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2) must be placed on the power supplies to provide a current pathway to ground.

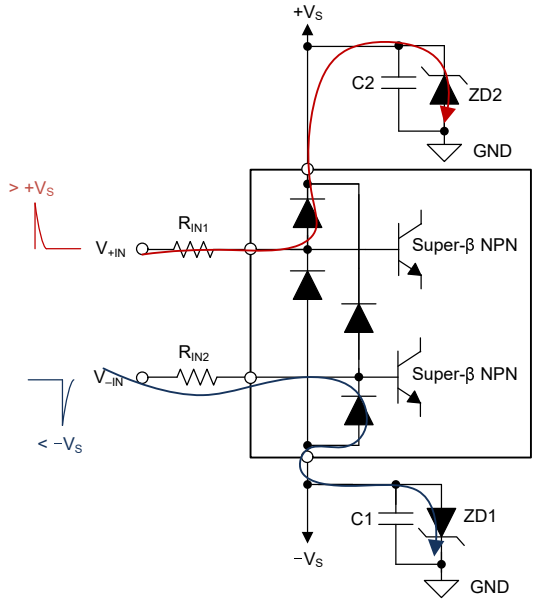


图 8-3. Input Current Path During an Overvoltage Condition

For an overvoltage condition, use an external resistor (R_{IN1}, R_{IN2}) to limit the current. The following equation gives the calculation for the protection resistors:

$$R_{IN1} = \frac{(V_{+IN}) - (+V_S)}{I_{MAX}} \quad (1)$$

where:

- V_{+IN} is the maximum input voltage
- $+V_S$ is the positive supply rail
- I_{MAX} is the maximum current allowed = 10 mA

Calclate R_{IN2} using the same method, substituting with V_{-IN}, $-V_S$, and $-I_{MAX}$.

Any additional resistance to the input pins adds more noise to the system. For more details, see 节 9.2.2.2.

8.4 Device Functional Modes

The INA848 has a single functional mode and is operational when the power supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the INA848 is 36 V (±18 V).

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9 Application and Implementation

Note

以下应用部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。客户应负责确定 TI 组件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

9.1.1 Filter Pin

The INA848 allows access between the two amplification stages. In applications surrounded from high input noise, adding filter stages can be of high benefit. 图 9-1 and 图 9-2 show two different filter scenarios that help filter out undesired differential signals.

9.1.1.1 RC Filter Network

In environments where known high-frequency noise must be eliminated, use a low-pass filter containing a capacitor, and optionally, a resistor.

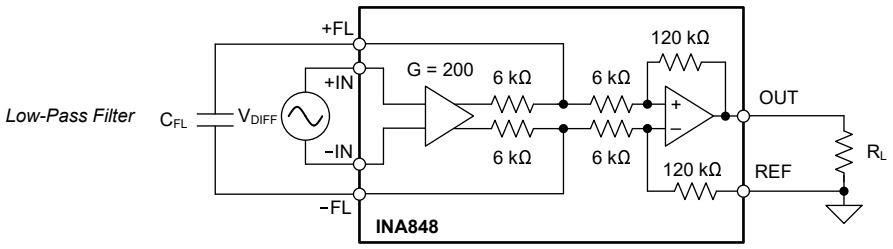


图 9-1. Low-pass Filter

The –3-dB cross frequency is determined given following equation:

$$f_{FL1} = \frac{1}{2\pi \cdot 6k\Omega \cdot C_{FL}} \quad (2)$$

Where 6 kΩ represents the internal resistor network. Use the Analog Engineer's Calculator for fast and easy bode plot visualization.

9.1.1.2 RLC Filter Network

In environments where a known, narrow-frequency band must be attenuated, a series LC filter network can be added between the filter pins, as shown in 图 9-2. The connection adds to the internal resistor network, and results in a RLC filter network that is also commonly known as bandstop filter.

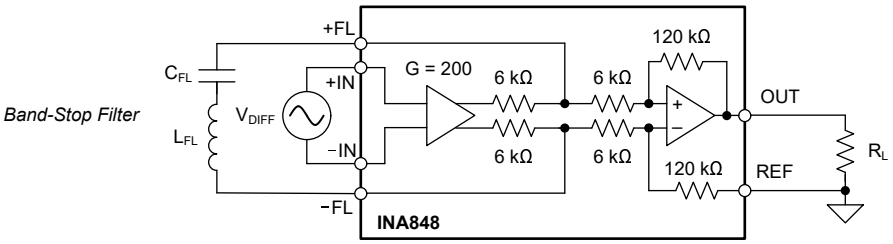


图 9-2. Bandstop Filter

Use 方程式 3 to calculate the middle frequency of the filter:

$$f_{FL2} = \frac{1}{2\pi \cdot \sqrt{(C_{FL} \cdot L_{FL})}} \quad (3)$$

In general, the width of the stopband is between one and two decades, meaning that the highest attenuation is between 10 to 100 around the middle frequency. This indication is commonly defined as the quality factor (Q factor) of the filter and is calculated by:

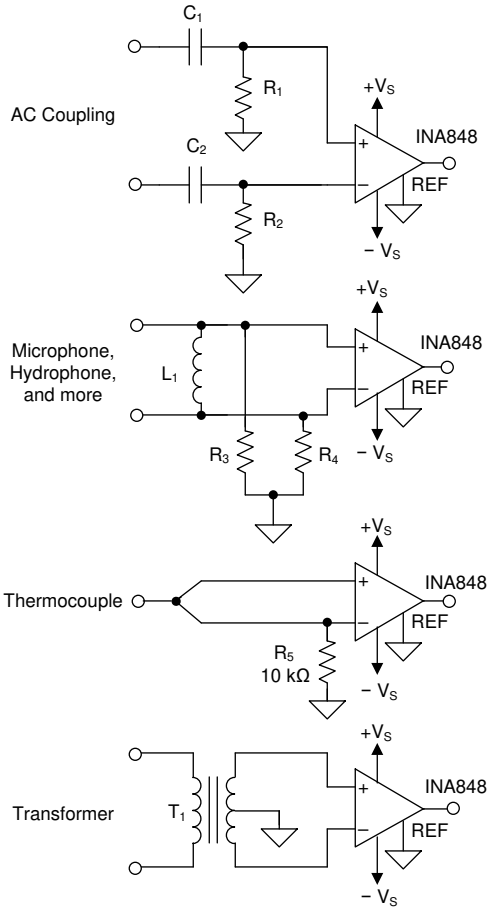
$$Q = \frac{1}{R} \cdot \sqrt{\frac{L_{FL}}{C_{FL}}} \tag{4}$$

The resistor is given by the internal resistor of 6 kΩ; therefore, the damping factor of the filter can further be affected of the series resistance of the inductor L_{FL}. For stable operation of the filter, choose an inductor in the range of 100 µH.

9.1.2 Input Bias Current Return Path

The input impedance of the INA848 is extremely high (approximately 100 GΩ). However, a path must be provided for the input bias current of both inputs. This input bias current is typically 25 nA. High input impedance means that this input bias current changes little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. 图 9-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA848, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path connects to one input (as shown in the thermocouple example in 图 9-3). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current, and better high-frequency common-mode rejection.



NOTE: Center tap in the transformer provides bias current return.

图 9-3. Providing an Input Common-Mode Current Path

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9.2 Typical Application

图 9-4 shows a typical application for the INA848.

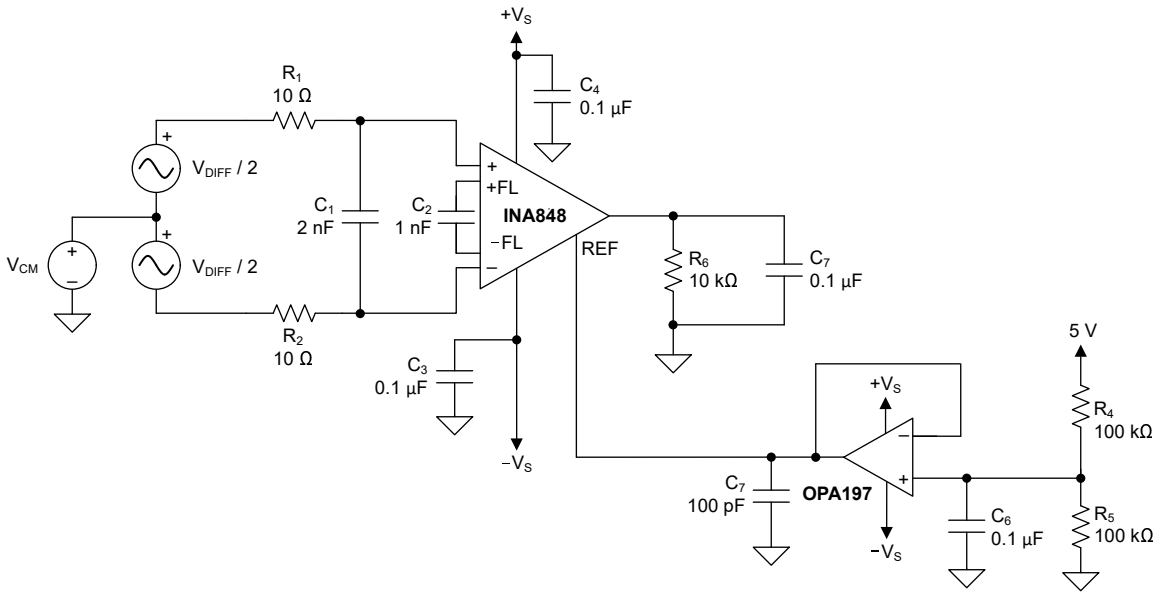


图 9-4. Sensor Conditioning (V_{DIFF} < 5 mV, $V_{S±}$ = 15 V)

9.2.1 Design Requirements

For this application, the design requirements are:

- Differential input signal of V_{DIFF} = 2.5 mV
- Common-mode input voltage of V_{CM} = 10 V
- Power-supply voltage of V_S = ± 15 V
- Reference voltage buffered to V_{REF} = 2.5 V
- Output range within 0 V to 5 V
- First-order filter stage with –3-dB frequency of 27 kHz

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9.2.2 Detailed Design Procedure

9.2.2.1 Reference Pin

The output voltage of the INA848 is developed with respect to the voltage on the reference pin (REF.)

The voltage source applied to the reference pin of the INA848 must have a low output impedance (R_{REF} > 5 Ω). Any additional resistance at the reference pin creates an imbalance in the four resistors of the internal difference amplifier, resulting in degraded common-mode rejection ratio (CMRR).

Voltage reference devices are an excellent option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider generates a reference voltage, the divider must be buffered by an op amp, as shown in 图 9-5, to avoid CMRR degradation.

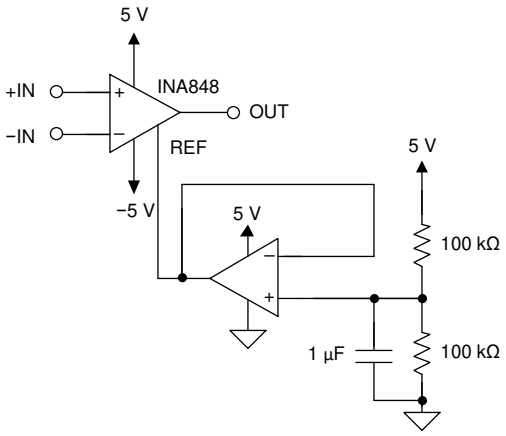


图 9-5. Buffer to drive the Reference Voltage

Often in dual-supply operation, the reference pin connects to the low-impedance system ground. The degradation effect of common-mode rejection ratio is thus neglegible as long as the output voltage (V_{OUT}) is referred to the reference pin (REF).

In single-supply operation, the output signal is offset to a precise midsupply level (for example, 2.5 V in a 5-V supply environment). In applications where the output voltage is offset to a reference voltage but referred to system ground, the degradation effect of common-mode rejection ratio must be considered.

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9.2.2.2 Noise Analysis

Low-noise instrumentation amplifiers such as the INA848 are designed to serve stringent and sensitive applications, such as surgical tools, microphones or other precision monitoring systems. A througough noise analysis is a key element in the design process.

TI`s super-beta transistors offer the benefits of low voltage noise and low current noise, thus allowing the INA848 excellent noise performance.

图 9-6 shows a simplified noise model including the gain stages of the INA848.

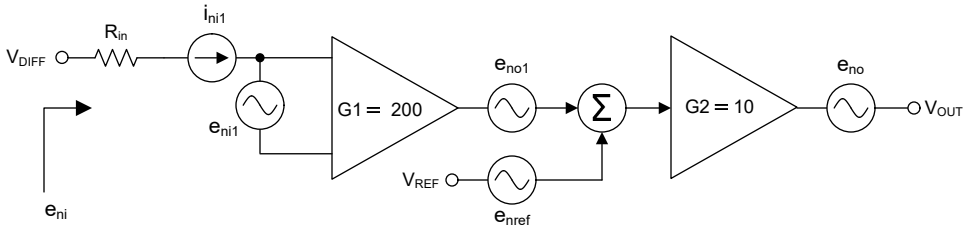


图 9-6. Simplified Noise Model

To get the total input-referred noise, e_{ni}, consider the source resistance seen by the positive and negative input pins of the instrumentation amplifier. The key elements that must be considered for a noise analysis in an instrumenation amplifier are:

- Current noise density $i_{ni1}$of the INA, see 节 7.5
- Voltage noise denisty e_{ni1} of the INA, see 节 7.5
- Voltage noise density caused by source resistance i_{ni}× R_{in}
- Resistor noise from source resistance e_{nRin} , given by: $\sqrt{Rin}$ × 4.04 nV/ $\sqrt{Hz}$
- Reference voltage noise e_{nref}

The noise sources are uncorrelated (that is, the noise signal is unpredictable). The result of mutliple uncorrelated noise sources is the square root of the sum of their squares (RSS). Thus, the total RTI noise density, e_{ni}, in nV/ $\sqrt{Hz}$ can be derived from the following equation:

$$e_{ni} = \sqrt{e_{ni1}^2 + e_{n(Rin)}^2 + (i_{ni1} \cdot R_{in})^2 + \left(\frac{e_{n(REF)}}{G1}\right)^2} \quad (5)$$

9.2.2.2.1 Reference Voltage Noise Contribution

图 9-7 shows the noise model of the reference buffer circuit given by 图 9-5 using the OPA197 amplifier.

To compute the total noise for the reference buffer circuit, consider the thermal noise of the divider (that is a parallel network from noise perspective), the amplifier voltage noise (that is, e_{nOPA} = 5.5 nV/ √Hz), and the voltage noise developed from the current noise of the amplifier (that is, i_{nOPA} = 1.5 fA/ √Hz) through the divider.

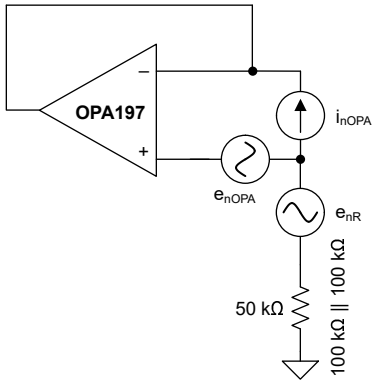


图 9-7. Reference Voltage Noise Model

Thus the total reference noise can be derived from following equation:

$$e_{n(REF)}=\sqrt{e_{nOPA}^2+(\sqrt{R}\cdot 4.04\ nV/\sqrt{Hz})^2+(i_{nOPA}\cdot R)^2} \quad (6)$$

The reference noise is divided by the first gain stage of 200 at the INA848 to compute the input-referred noise. For reference noise less than 80 nV/ √Hz, this contribution can be neglected in the analysis. The given example results in a total reference noise of 29 nV/ √Hz, and thus is neglected.

9.2.3 Application Curves

From 图 9-6, the source resistance is shown to be one main contributor. 图 9-8 plots all the individual noise contributors depending on the source resistance. The reference voltage noise is neglegible.

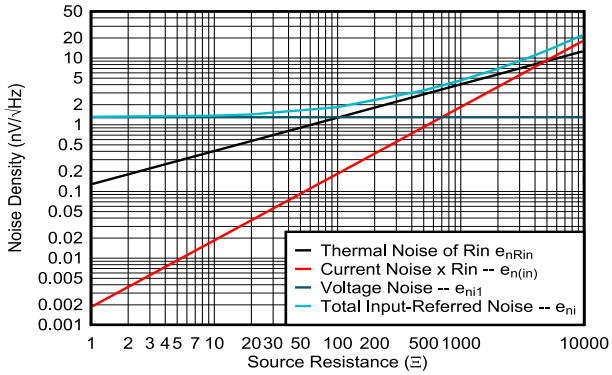


图 9-8. Noise Density vs Source Resistance

If the source resistance is below 20 Ω, the voltage noise of the INA (typically 1.3 nV/ √Hz) is dominating. If the source resistance is increasing (> 20 Ω) the thermal noise of the source resistance is dominating. At this point the low-noise advantage of the INA848 does not provide additional value. In applications with even higher source resistance (> 1 kΩ), the current noise of the INA starts to dominate, and thus, should be optimized.

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10 Power Supply Recommendations

The nominal performance of the INA848 is specified with a supply voltage of ±15 V and midsupply reference voltage. The device operates using power supplies from ±4 V (8 V) to ±18 V (36 V) and non-midsupply reference voltages with excellent performance.

CAUTION

Supply voltages higher than 40 V (±20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in 节 *7.6* of this data sheet.

11 Layout

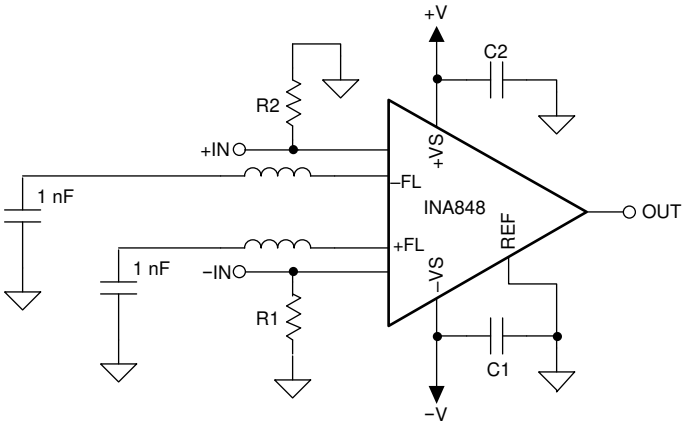
11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Take care to make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from +VS to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components (filter components, load) as close to the device as possible.
- Use ground layer to minimize the parasitic inductance of the board.
- Keep the traces as short as possible.

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11.2 Layout Example



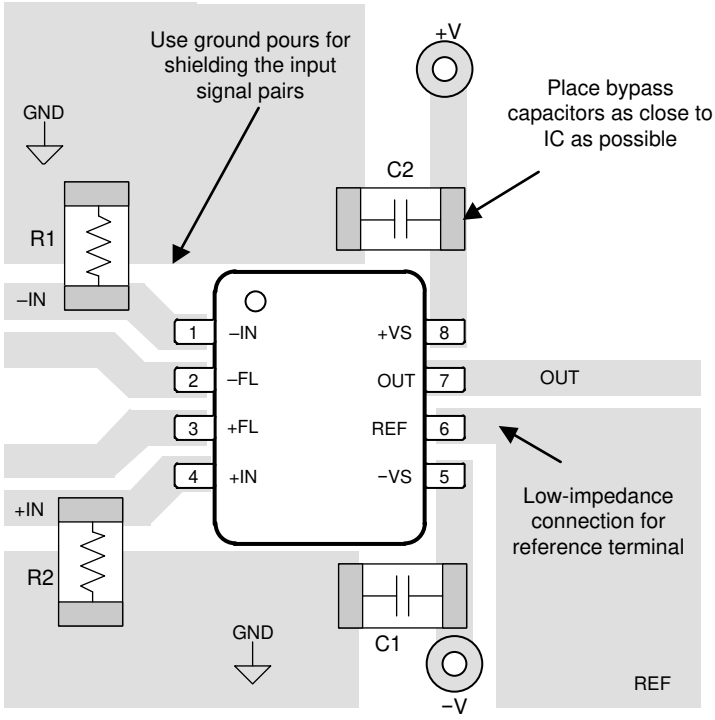


图 11-1. Example Schematic and Associated PCB Layout (inductors and capacitors shown on FL pins are optional)

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference*
- Texas Instruments, *OPA191 Low-Power, Precision, 36-V, e-trim CMOS Amplifier*
- Texas Instruments, TINA-TI software folder
- Texas Instruments, INA Common-Mode Range Calculator

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

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12.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA848ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA848
INA848ID.Z	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA848
INA848IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA848
INA848IDR.Z	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA848

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

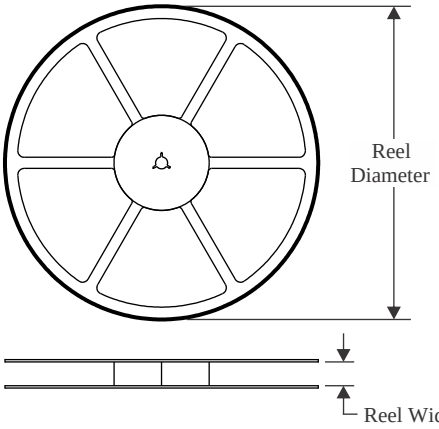
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

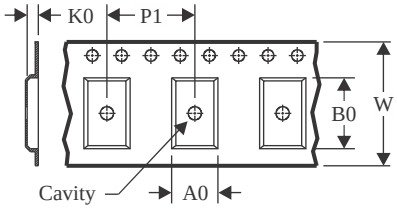
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

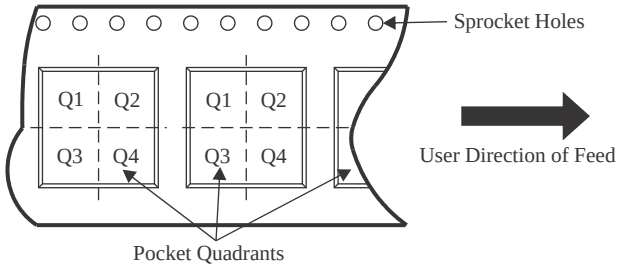


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

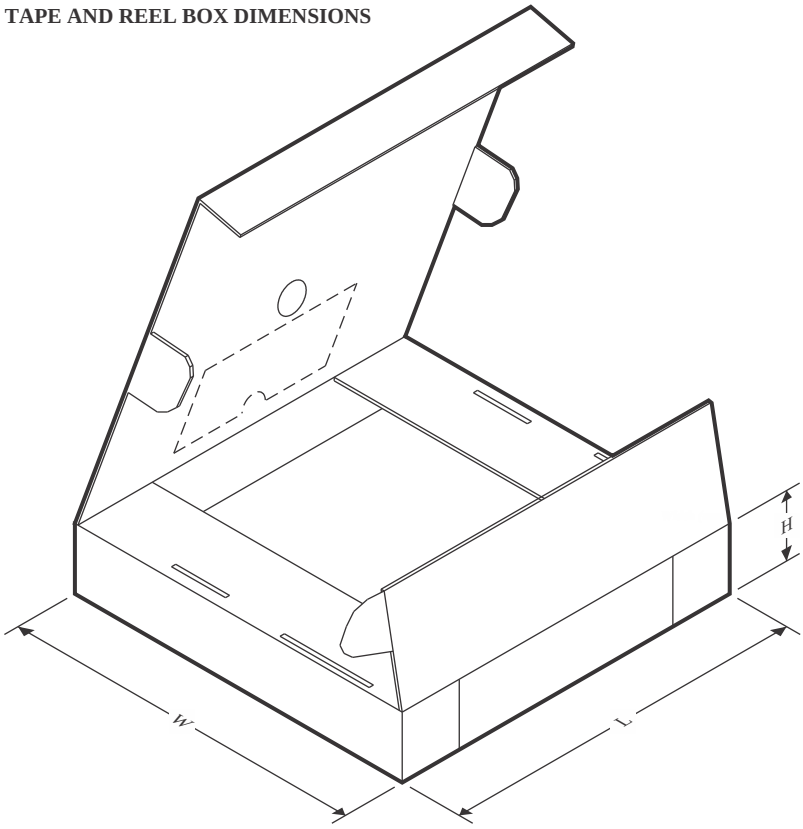
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA848IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

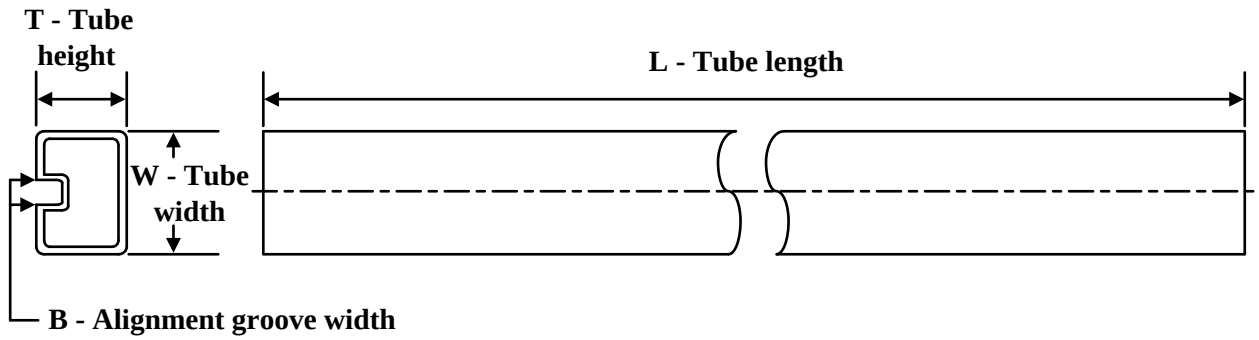
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

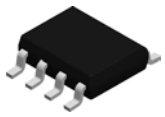
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA848IDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA848ID	D	SOIC	8	75	506.6	8	3940	4.32
INA848ID.Z	D	SOIC	8	75	506.6	8	3940	4.32

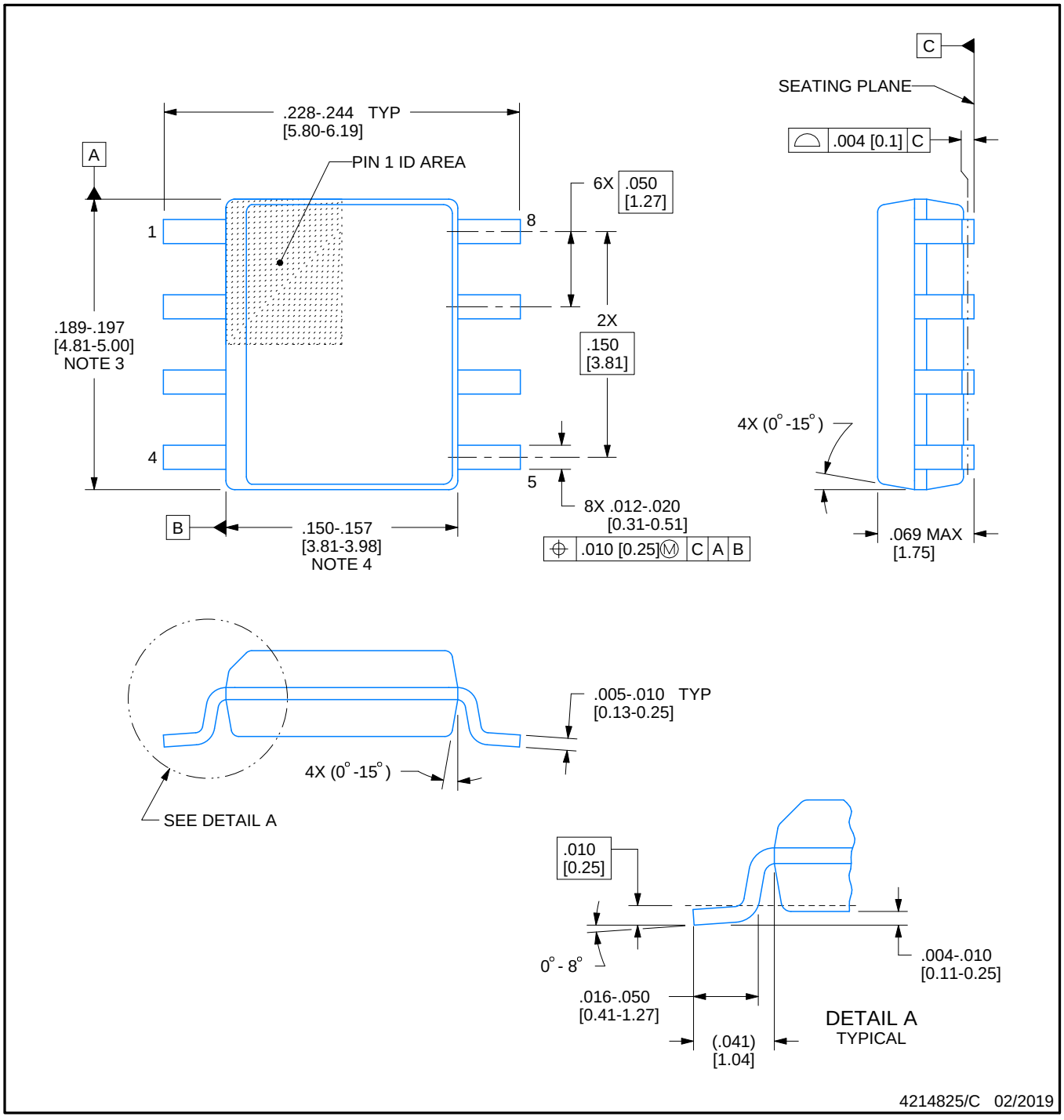


PACKAGE OUTLINE

D0008A

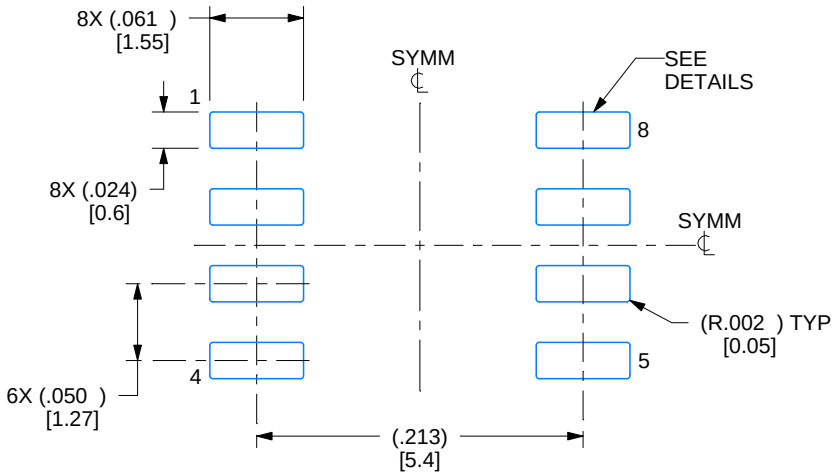
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

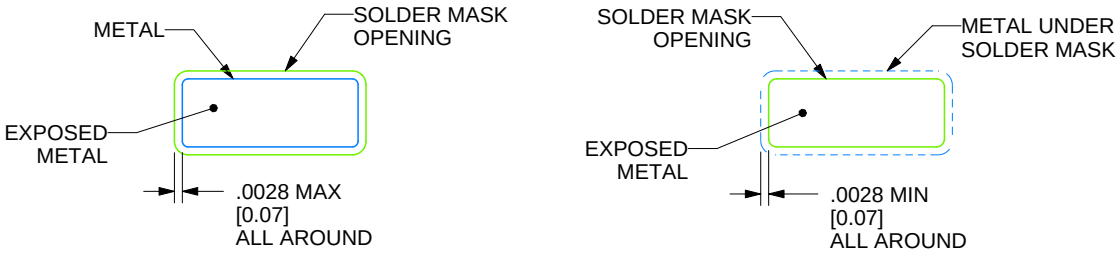


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

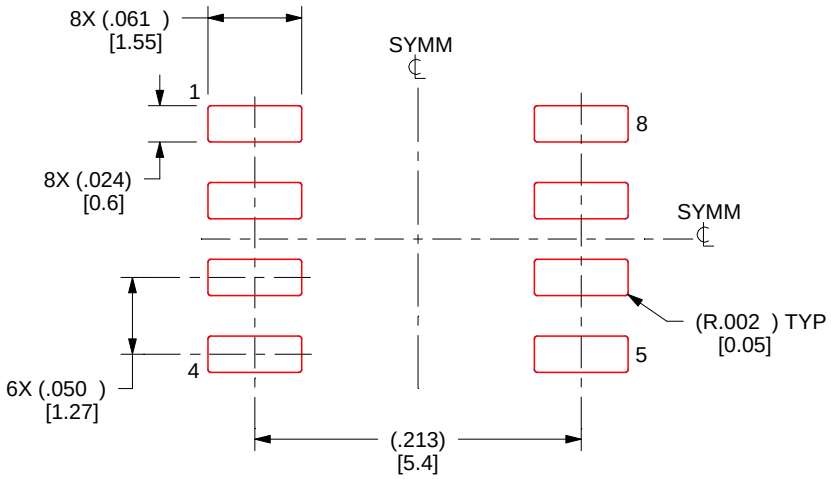
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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