XCL104/XCL105 Series

ETR28031-001a

1.4A, Inductor Built-in Step-up DC/DC Converters

☆Green Operation compatible

■GENERAL DESCRIPTION

XCL104/XCL105 series are synchronous step-up DC/DC converters which integrates an inductor with a 0.17Ω Nch driver FET and a 0.23Ω synchronous Pch switching FET built-in.

The series are able to start operation from an input voltage of 0.9V, suitable for equipment using single Alkaline battery or Nickel metal hydride battery.

The output voltage can be set from 1.8V to 5.5V in steps of 0.1V.

During the devices enter stand-by mode, A/D/G/J types prevent the application malfunction by C_L Discharge function which can quickly discharge the electric charge at the output capacitor (C_L). B/E/H/K types are able to allows the drive of subsequent devices by the bypass function which maintain continuity between the input and output. C/F/M/L types are able to connect in output voltage OR circuit with other power supplies by Load Disconnection function which breaks continuity between the input and output.

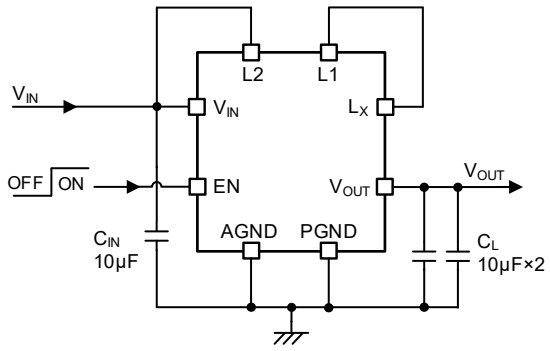
■APPLICATIONS

- ●Portable equipment
- ●Beauty & health equipment
- ●Wearable devices
- ●Game & Hobby
- ●PC Peripherals
- ●Devices with 1~3 Alkaline, 1~3 Nickel Hydride, 1 Lithium and 1 Li-ion

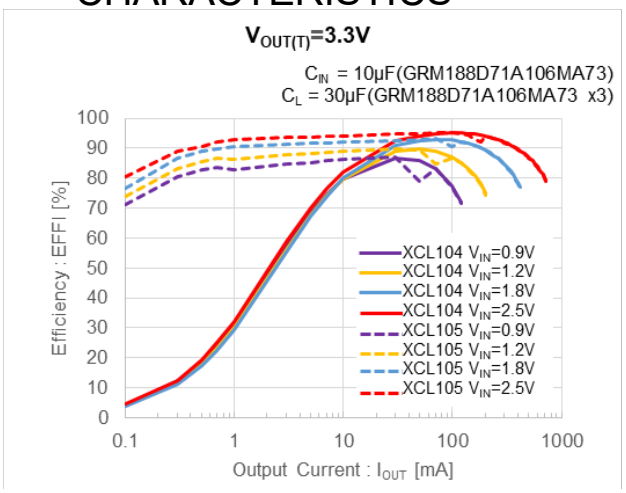
■FEATURES

Input Voltage Range	: 0.65V ~ 6.0V (Operation start voltage : 0.9V)
Fixed Output Voltage	: 1.8V ~ 5.5V (A,B,C type)
	: 2.2V ~ 5.5V (except A,B,C type)
Oscillation Frequency	: 1.2MHz
Output Current	: 710mA @V_{OUT}=5.0V, V_{IN}=3.3V
	420mA @V_{OUT}=3.3V, V_{IN}=1.8V
Control Mode Selection	: PWM (XCL104)
	PWM/PFM (XCL105)
Load Transient Response	: 120mV@V_{OUT}=3.3V, V_{IN}=1.8V, f_{osc}=1.2MHz
	I_{OUT}=1mA→200mA (tr=5μs)
Protection Function	: Thermal shutdown
	Current limit
	Integral latch method (D/E/F/J/K/L types)
	Short circuit protection (D/E/F/J/K/L types)
	UVLO (G/H/M/J/K/L types)
Functions	: Soft-start
	Load Disconnection (A/C/D/F/G/M/J/L types)
	C_L Auto Discharge (A/D/G/J types)
	Bypass Switch (XCL105 B/E/H/K types)
Output Capacitor	: Ceramic Capacitor
Operating Ambient Temperature	: -40℃ ~ 105℃
Package	: DFN3030-10B (3.0x3.0x1.7mm)
Environmentally Friendly	: EU RoHS Compliant, Pb Free

■TYPICAL APPLICATIONS CIRCUIT

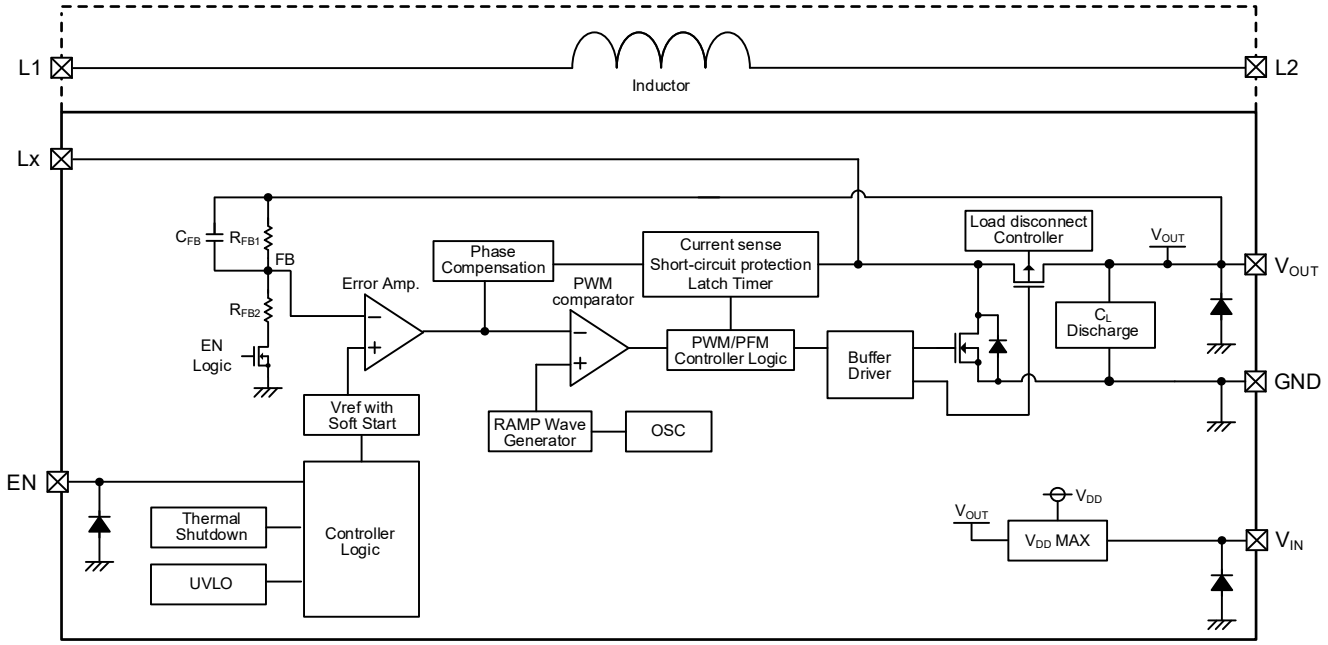


■TYPICAL PERFORMANCE CHARACTERISTICS



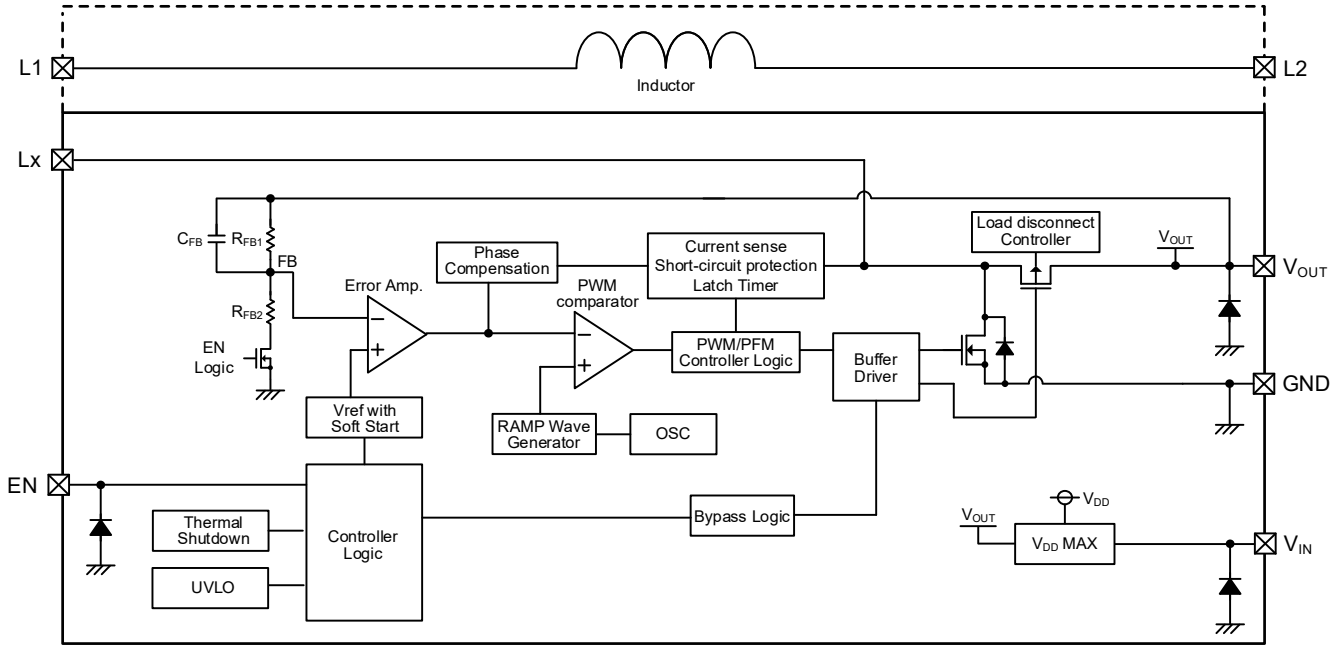
■BLOCK DIAGRAM

● XCL104/XCL105 A/D/G/J types



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.
XCL104 series chooses only PWM control.
UVLO / short circuit protection / integral latch can be selected according to the types.

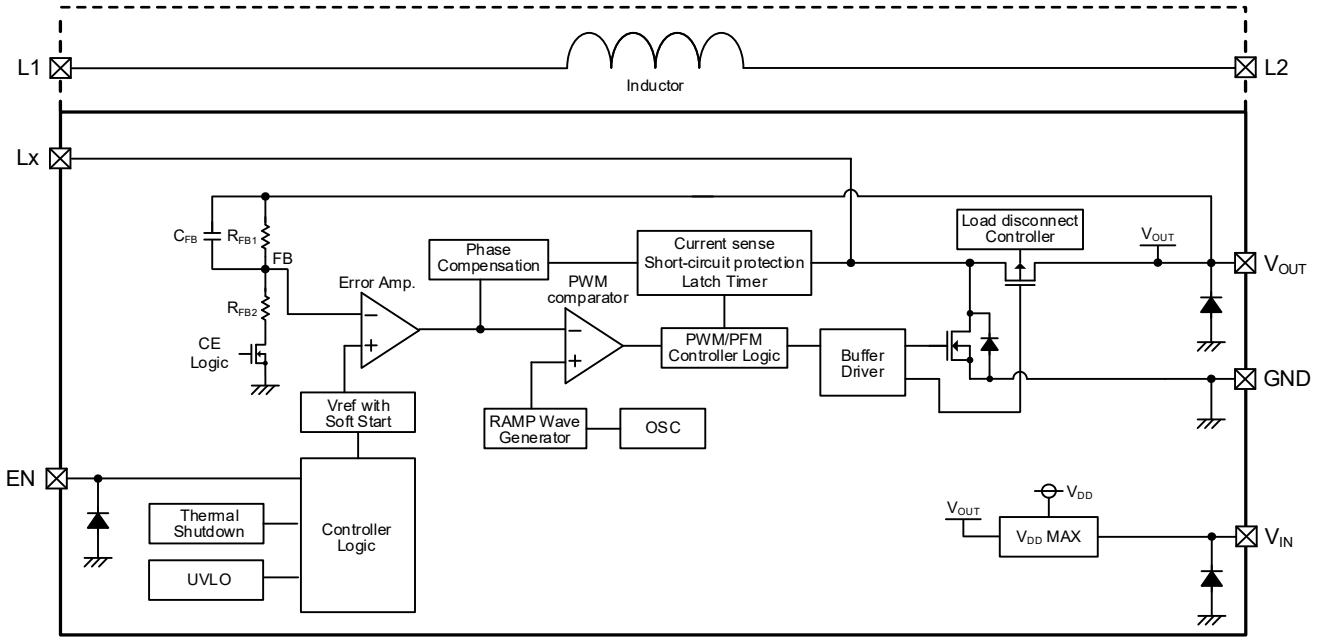
● XCL105 B/E/H/K types



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.
UVLO / short circuit protection / integral latch can be selected according to the types.

■BLOCK DIAGRAM

●XCL105 C/F/M/L types



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.
UVLO / short circuit protection / integral latch can be selected according to the types.

■PRODUCT CLASSIFICATION

1. Standard product

●Ordering Information

XCL104①②③④⑤⑥-⑦ : PWM Control

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	A	Refer to Selection Guide
		D	
②③	Output Voltage (A Type)	18 ~ 55	Output Voltage : e.g. V_{OUT}=1.8V⇒②=1, ③=8 Output Voltage Range: 1.8V ~ 5.5V (0.1V increments)
	Output Voltage (D Type)	22 ~ 55	Output Voltage : e.g. V_{OUT}=2.5V⇒②=2, ③=5 Output Voltage Range: 2.2V ~ 5.5V (0.1V increments)
④	Oscillation Frequency	1	1.2MHz
⑤⑥-⑦(*1)	Package (Order Unit)	H2-G	DFN3030-10B (3,000pcs/Reel)

(*1) The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully EU RoHS compliant.

Selection Guide

TYPE	Purpose	UVLO	C_L Discharge	Current Limit	Short Protection	Stand-by Options at EN="L"
A	Load Disconnection	-	Yes	Yes (Without latch)	-	Complete Output Disconnect
D				Yes (With integral latch)	Yes	

●Ordering Information

XCL105①②③④⑤⑥-⑦ : PWM/PFM automatic switching control

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	A	Refer to Selection Guide
		B	
		C	
		D	
②③	Output Voltage (A/B/C Type)	18 ~ 55	Output Voltage : e.g. V_{OUT}=1.8V⇒②=1, ③=8 Output Voltage Range: 1.8V ~ 5.5V (0.1V increments)
	Output Voltage (D Type)	22 ~ 55	Output Voltage : e.g. V_{OUT}=2.5V⇒②=2, ③=5 Output Voltage Range: 2.2V ~ 5.5V (0.1V increments)
④	Oscillation Frequency	1	1.2MHz
⑤⑥-⑦(*1)	Package (Order Unit)	H2-G	DFN3030-10B (3,000pcs/Reel)

(*1) The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully EU RoHS compliant.

Selection Guide

TYPE	Purpose	UVLO	C_L Discharge	Current Limit	Short Protection	Stand-by Options at EN="L"
A	Load Disconnection	-	Yes	Yes (Without latch)	-	Complete Output Disconnect
D				Yes (With integral latch)	Yes	
B	Bypass Mode at EN="L"	-	-	Yes (Without latch)	-	Input-to-Output Bypass
C	V_{OUT} OR Connection	-	-	Yes (Without latch)	-	Complete Output Disconnect

■PRODUCT CLASSIFICATION

2. Custom product (*1)

(*1) Please contact our sales representative if you wish to select a custom product.

●Ordering Information

XCL104①②③④⑤⑥-⑦ : PWM Control

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	G	Refer to Selection Guide
		J	
②③	Output Voltage (G/J Type)	22 ~ 55	Output Voltage : e.g. V_{OUT}=2.5V⇒②=2, ③=5 Output Voltage Range: 2.2V ~ 5.5V (0.1V increments)
④	Oscillation Frequency	1	1.2MHz
⑤⑥–⑦(*2)	Package (Order Unit)	H2-G	DFN3030-10B (3,000pcs/Reel)

(*1) The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully EU RoHS compliant.

Selection Guide

TYPE	Purpose	UVLO	C_L Discharge	Current Limit	Short Protection	Stand-by Options at EN="L"
G	Load Disconnection	Yes	Yes	Yes (Without latch)	-	Complete Output Disconnect
J				Yes (With integral latch)	Yes	

■PRODUCT CLASSIFICATION

2. Custom product (*1) (Continued)

(*1) Please contact our sales representative if you wish to select a custom product.

●Ordering Information

XCL105①②③④⑤⑥-⑦ : PWM/PFM automatic switching control

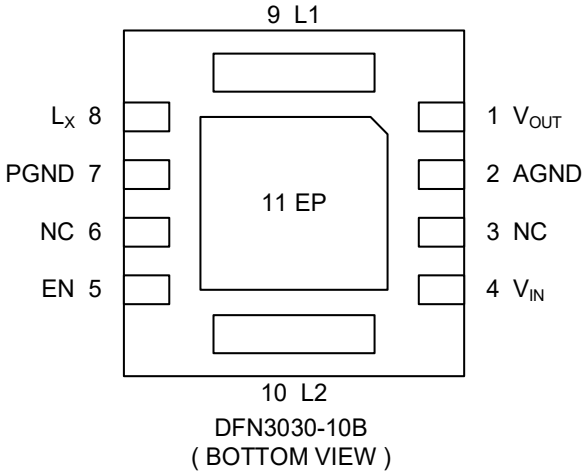
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	E	Refer to Selection Guide
		F	
		G	
		H	
		J	
		K	
		L	
		M	
②③	Output Voltage (E/F/G/H/M/J/K/L Type)	22 ~ 55	Output Voltage : e.g. V_{OUT}=2.5V⇒②=2, ③=5 Output Voltage Range: 2.2V ~ 5.5V (0.1V increments)
④	Oscillation Frequency	1	1.2MHz
⑤⑥-⑦(*2)	Packages (Order Unit)	H2-G	DFN3030-10B (3,000pcs/Reel)

(*1) The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully EU RoHS compliant.

Selection Guide

TYPE	Purpose	UVLO	C_L Discharge	Current Limit	Short Protection	Stand-by Options at EN="L"
G	Load Disconnection	Yes	Yes	Yes (Without latch)	-	Complete Output Disconnect
J				Yes (With integral latch)	Yes	
E	Bypass Mode at EN="L"	-	-	Yes (With integral latch)	Yes	Input-to-Output Bypass
H		Yes		Yes (Without latch)	-	
K				Yes (With integral latch)	Yes	
F	V_{OUT} OR Connection	-	-	Yes (With integral latch)	Yes	Complete Output Disconnect
M		Yes		Yes (Without latch)	-	
L				Yes (With integral latch)	Yes	

■PIN CONFIGURATION



DFN3030-10B
(BOTTOM VIEW)

■PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTIONS
1	V_{OUT}	Output Voltage
2	AGND	Analog Ground
3	NC	No Connection
4	V_{IN}	Power Input
5	EN	Enable
6	NC	No Connection
7	PGND	Power Ground
8	L_X	Switching
9	L1	Inductor Electrodes
10	L2	Inductor Electrodes
11	EP	Exposed thermal pad. The Exposed pad must be connected to GND(Pin2,7).

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
EN	L	Stand-by
	H	Active
	OPEN	Undefined State (*1)

(*1) Do not leave the EN pin open.

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER	SYMBOL	RATINGS	UNITS
V_{IN} Pin Voltage	V_{IN}	-0.3 ~ 7.0	V
Lx Pin Voltage	V_{Lx}	-0.3 ~ 7.0	V
V_{OUT} Pin Voltage	V_{OUT}	-0.3 ~ 7.0	V
EN Pin Voltage	V_{EN}	-0.3 ~ 7.0	V
Power Dissipation (Ta=25℃)	Pd	1950 (JESD51-7 board) (*1)	mW
Junction Temperature	Tj	-40 ~ 125	℃
Storage Temperature	Tstg	-55 ~ 125	℃

GND(AGND,PGND) are standard voltage for all of the voltages.

(*1) The power dissipation figure shown above is based upon PCB mounted and it is for reference only.
Please refer to PACKAGING INFORMATION for the mounting condition.

■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Voltage	V_{IN}	-	-	6.0	V
Applied voltage to V_{OUT} (*1)	V_{OUT}	$V_{OUT(T)}$	-	6.0	V
Lx Pin Current (*2)	I_{LX}	-	-	3.5	A
EN Pin Voltage	V_{EN}	0.0	-	6.0	V
Operating Ambient Temperature	Topr	-40	-	105	℃
Junction Temperature	Tj	-40	-	125	℃
Input Capacitor (Effective Value)	C_{IN}	3.3 (*3)	-	1000 (*4)	μF

GND(AGND,PGND) are standard voltage for all of the voltage.

$V_{OUT(T)}$: Target Output voltage

(*1) Depending on the type of product and operation mode, some external voltages cannot be applied to the output side. Regarding to support for OR connection or not, please refer to the operational explanation and NOTES ON USE.

(*2) Due to the Lx pin current, the junction temperature may cross over the maximum junction temperature. Please use within the range that does not cross over the maximum junction temperature.

(*3) Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

(*4) If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitance, place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase and the IC may malfunction.

■ELECTRICAL CHARACTERISTICS

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS	CIRCUIT
Input Voltage	V_{IN}			-	-	6.0	V	−
Output Voltage	V_{OUT}	Voltage to start oscillation while $V_{OUT}=V_{OUT(T)}$ ×1.03→$V_{OUT(T)}$×0.97		<E-1>	<E-2>	<E-3>	V	⑤
Operation Start Voltage	V_{ST1}	R_L=OPEN	A/B/C/D/E/F Type	-	-	0.90	V	①
Operation Hold Voltage	V_{HLD}	R_L=OPEN	A/B/C/D/E/F Type	-	0.65	-	V	①
Quiescent Current (XCL105)	Iq	$V_{IN}=V_{OUT(T)}+0.2V$ $V_{OUT}=V_{OUT(T)}+0.5V$		-	19.0	38.0	μA	③
Input Pin Quiescent Current	Iq_in	V_{IN}= $V_{OUT(T)}$-0.2V, V_{OUT}= $V_{OUT(T)}$+0.5V	XCL105 C/F	-	0.12	0.36	μA	③
			XCL105 M/L	-	1.20	2.06		
Oscillation Frequency	f_{OSC}	V_{IN}=1.7V, V_{OUT}=1.7V		1.02	1.20	1.38	MHz	⑤
Maximum Duty Cycle	D_{MAX}	V_{IN}=1.7V, V_{OUT}=1.7V		85	91	98	%	⑤
Minimum Duty Cycle	D_{MIN}	$V_{OUT}=V_{IN}$= $V_{OUT(T)}$+0.5V		-	-	0	%	⑤
PFM Switching Current (XCL105)	I_{PFM}	V_{IN}=1.7V, R_L: OPEN		-	280	500	mA	①
Stand-by Current	I_{STB}	$V_{IN}=V_{Lx}$=6.0V, V_{EN}=0.0V(*1)	A/D/G/J Type	-	0.0	1.0	μA	⑧
			B/E/H/K Type	-	0.0	1.0	μA	⑦
			C/F/M/L Type	-	0.16	1.0	μA	⑧
Lx SW "Nch" ON Resistance	R_{LXN}	V_{IN}=3.3V, V_{OUT}=1.7V		-	0.17 (*3)	-	Ω	-
Lx SW "Pch" ON Resistance	R_{LXP}	$V_{IN}=V_{Lx}$=3.3V, I_{OUT}=200mA		-	0.23 (*2)	-	Ω	④
Lx SW ”H” Leakage Current	I_{LXLH}	V_{IN}=6.0V, V_{EN}=0V, V_{Lx}=6.0V(*1)	A/C/D/F/G/M/J/L Type	-	0.0	1.0	μA	⑧
			B/E/H/K Type					⑦
Lx SW ”L” Leakage Current (XCL105 C/F/M/L)	I_{LXLL}	V_{IN}=0.0V, V_{EN}=0.0V, V_{Lx}=0.0V, V_{OUT}=6.0V		-	0.0	1.0	μA	②
Current Limit	I_{LIM}	V_{IN}= $V_{OUT(T)}$-0.2V, R_{Lx}=0.5Ω		<E-4>	<E-5>	<E-6>	A	⑥
Integral Latch Time (D/E/F/J/K/L Type)	t_{LAT}	V_{IN}= $V_{OUT(T)}$-0.3V, R_{Lx}=0.5Ω, Time from current limit start to stop Lx oscillation		45	200	450	μs	⑥
Latch Release Voltage (D/E/F Type)	V_{LAT_R}	After the integral latch was operated, R_L:OPEN, $V_{IN}=V_{OUT(T)}$-0.2V→0.9V		0.9	1.2	1.5	V	①
Short-circuit Protection Threshold Voltage (D/E/F/J/K/L Type)	V_{SHORT}	$V_{IN}=V_{OUT(T)}$-0.2V, R_L=0Ω		-	V_{IN}(*3)	-	V	①

■ELECTRICAL CHARACTERISTICS (Continued)

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS	CIRCUIT
Soft-Start Time	t_{SS}	V_{IN}= $V_{OUT(T)}$×0.85, V_{OUT} =$V_{OUT(T)}$× 0.9, After "H" is fed to EN, the time by when clocks are generated at Lx pin.		0.58	1.20	2.50	ms	⑤
C_L Discharge Resistance (A/D/G/J Type)	R_{DCHG}	V_{IN}= 3.3V, V_{OUT}=3.3V, V_{EN}=0V		100	180	400	Ω	②
EN "H" Voltage	V_{ENH}	V_{OUT}= $V_{OUT(T)}$-0.15V, Applied voltage to V_{EN}, Voltage changes Lx to be generated.	Ta=25℃	0.80	-	6.00	V	⑤
			Ta=-40 ~105℃(*3)	0.80	-	6.00		
EN "L" Voltage	V_{ENL}	V_{OUT}= $V_{OUT(T)}$-0.15V, Applied voltage to V_{EN}, Voltage changes Lx to “H” level	Ta=25℃	GND	-	0.20	V	⑤
			Ta=-40 ~105℃(*3)	GND	-	0.20		
EN "H" Current	I_{ENH}	V_{IN}=6.0V, V_{OUT}=6.0V, V_{Lx}=6.0V, V_{EN}=6.0V		-0.1	0.0	0.1	μA	②
EN "L" Current	I_{ENL}	V_{IN}=6.0V, V_{OUT}=6.0V, V_{Lx}=6.0V, V_{EN}=0.0V		-0.1	0.0	0.1	μA	②
Thermal Shutdown Temperature	T_{TSD}			-	150	-	℃	−
Hysteresis Width	T_{HYS}			-	25	-	℃	−
UVLO Release Voltage (G/H/M/J/K/L Type)	V_{UVLO_R}	R_L=1kΩ, While V_{IN}=0.2V→1.8V, Voltage to start oscillation		1.40	1.60	1.73	V	①
UVLO Hysteresis Width (G/H/M/J/K/L Type)	V_{UVLO_HYS}			0.070	0.150	0.215	V	①
UVLO Detect Delay (G/H/M/J/K/L Type)	t_{DF}	After V_{IN}=($V_{OUT(T)}$+V_{UVLO_R})/2→0.65V, time to stop oscillation		52	200	425	μs	①
Inductance Value	L	Test Frequency=1MHz		-	4.7	-	μH	−

Test conditions : unless otherwise stated, V_{IN}=1.5V, V_{EN}=3.3V, Lx=OPEN, R_{Lx}=56Ω

$V_{OUT(T)}$: Target voltage

(*1) A/C/D/F/G/M/J/L types : V_{OUT}=0.0V

B/E/H/K types : V_{OUT}=OPEN

(*2) Design value of A/C/D/F/G/M/J/L types

(*3) Design value

Table 1. External Components R_L Table

$V_{OUT(T)}$	R_L
1.8V≦$V_{OUT(T)}$<2.1V	150Ω
2.1V≦$V_{OUT(T)}$<3.1V	220Ω
3.1V≦$V_{OUT(T)}$<4.3V	330Ω
4.3V≦$V_{OUT(T)}$≦5.5V	470Ω

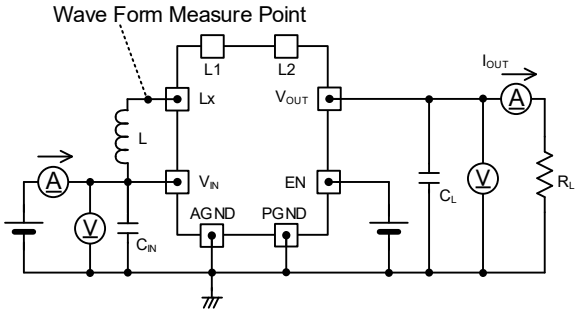
■ELECTRICAL CHARACTERISTICS (Continued)

Table 2. SPEC Table

NOMINAL OUTPUT VOLTAGE	V_{OUT}			I_{LIM}		
	<E-1>	<E-2>	<E-3>	<E-4>	<E-5>	<E-6>
UNITS	V	V	V	A	A	A
$V_{OUT(T)}$	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
1.8	1.764	1.800	1.836	-	1.28	3.10
1.9	1.862	1.900	1.938	-	1.47	3.10
2.0	1.960	2.000	2.040	-	1.65	3.10
2.1	2.058	2.100	2.142	-	1.81	3.10
2.2	2.156	2.200	2.244	-	1.95	3.10
2.3	2.254	2.300	2.346	-	2.07	3.10
2.4	2.352	2.400	2.448	-	2.17	3.10
2.5	2.450	2.500	2.550	-	2.26	3.10
2.6	2.548	2.600	2.652	-	2.32	3.10
2.7	2.646	2.700	2.754	-	2.37	3.10
2.8	2.744	2.800	2.856	-	2.40	3.10
2.9	2.842	2.900	2.958	-	2.41	3.10
3.0	2.940	3.000	3.060	1.52	2.42	3.10
3.1	3.038	3.100	3.162	1.52	2.42	3.10
3.2	3.136	3.200	3.264	1.52	2.42	3.10
3.3	3.234	3.300	3.366	1.53	2.42	3.10
3.4	3.332	3.400	3.468	1.53	2.42	3.10
3.5	3.430	3.500	3.570	1.54	2.42	3.10
3.6	3.528	3.600	3.672	1.54	2.42	3.10
3.7	3.626	3.700	3.774	1.54	2.42	3.10
3.8	3.724	3.800	3.876	1.55	2.42	3.10
3.9	3.822	3.900	3.978	1.55	2.42	3.10
4.0	3.920	4.000	4.080	1.55	2.42	3.10
4.1	4.018	4.100	4.182	1.56	2.42	3.10
4.2	4.116	4.200	4.284	1.56	2.42	3.10
4.3	4.214	4.300	4.386	1.57	2.42	3.10
4.4	4.312	4.400	4.488	1.57	2.42	3.10
4.5	4.410	4.500	4.590	1.57	2.42	3.10
4.6	4.508	4.600	4.692	1.58	2.42	3.10
4.7	4.606	4.700	4.794	1.58	2.42	3.10
4.8	4.704	4.800	4.896	1.58	2.42	3.10
4.9	4.802	4.900	4.998	1.59	2.42	3.10
5.0	4.900	5.000	5.100	1.59	2.42	3.10
5.1	4.998	5.100	5.202	1.59	2.42	3.10
5.2	5.096	5.200	5.304	1.60	2.42	3.10
5.3	5.194	5.300	5.406	1.60	2.42	3.10
5.4	5.292	5.400	5.508	1.61	2.42	3.10
5.5	5.390	5.500	5.610	1.61	2.42	3.10

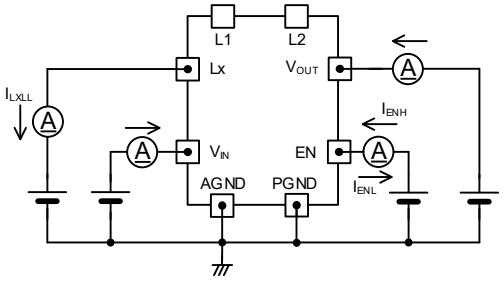
■TEST CIRCUITS

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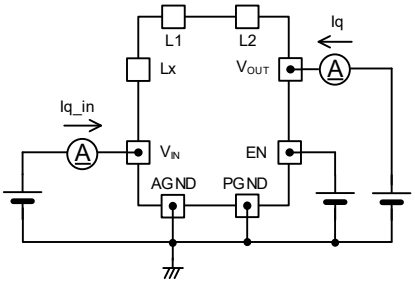


※External Components
C_{IN} : 10μF(ceramic)
L : 4.7μH
C_L : 30μF(ceramic)

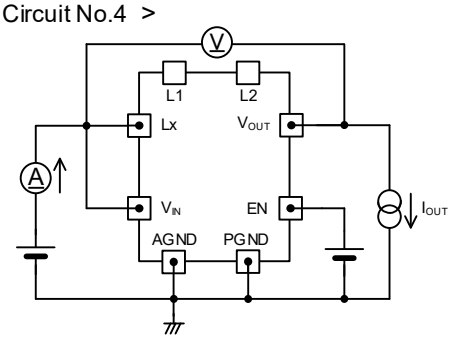
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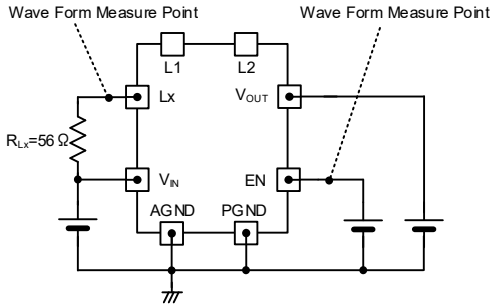
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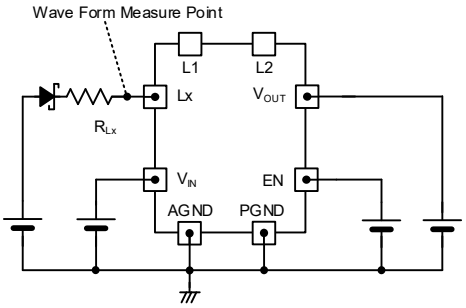
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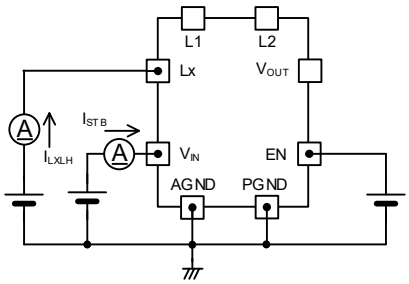
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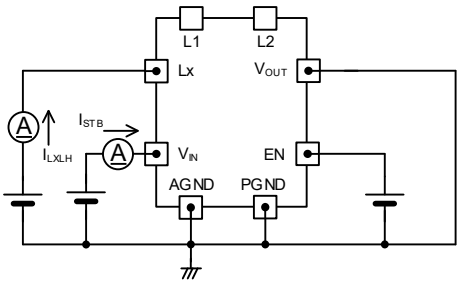
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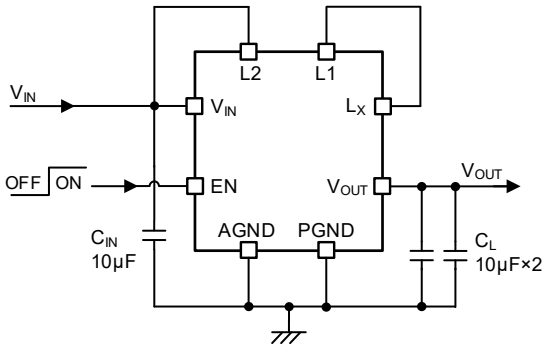
< Circuit No.7 >



< Circuit No.8 >



■TYPICAL APPLICATION CIRCUIT / PARTS SELECTION GUIDE



【Typical Examples】

	CONDITIONS	MANUFACTURER	PRODUCT NUMBER	VALUE	SIZE(L×W×T)
C_{IN}(*1)	-	Murata	GRM188D71A106MA73	10μF/10V	1.6x0.8x0.8mm
C_L(*2)	Input Current≦1.0A	Murata	GRM188D71A106MA73	10μF/10V x 2	1.6x0.8x0.8mm
	1.0A< Input Current	Murata	GRM188D71A106MA73	10μF/10V x 3	1.6x0.8x0.8mm

(*1) Use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

(*2) If a tantalum or low ESR electrolytic capacitor is used for the C_L, the ripple voltage will increase.
When using an electrolytic capacitor for the C_L, connect a ceramic capacitor in parallel before use.

In addition, when a large-capacity ceramic capacitor, tantalum, low ESR electrolytic capacitor, etc. are used for the C_L, the following operations may occur.

(a) The output voltage may become unstable under heavy load.

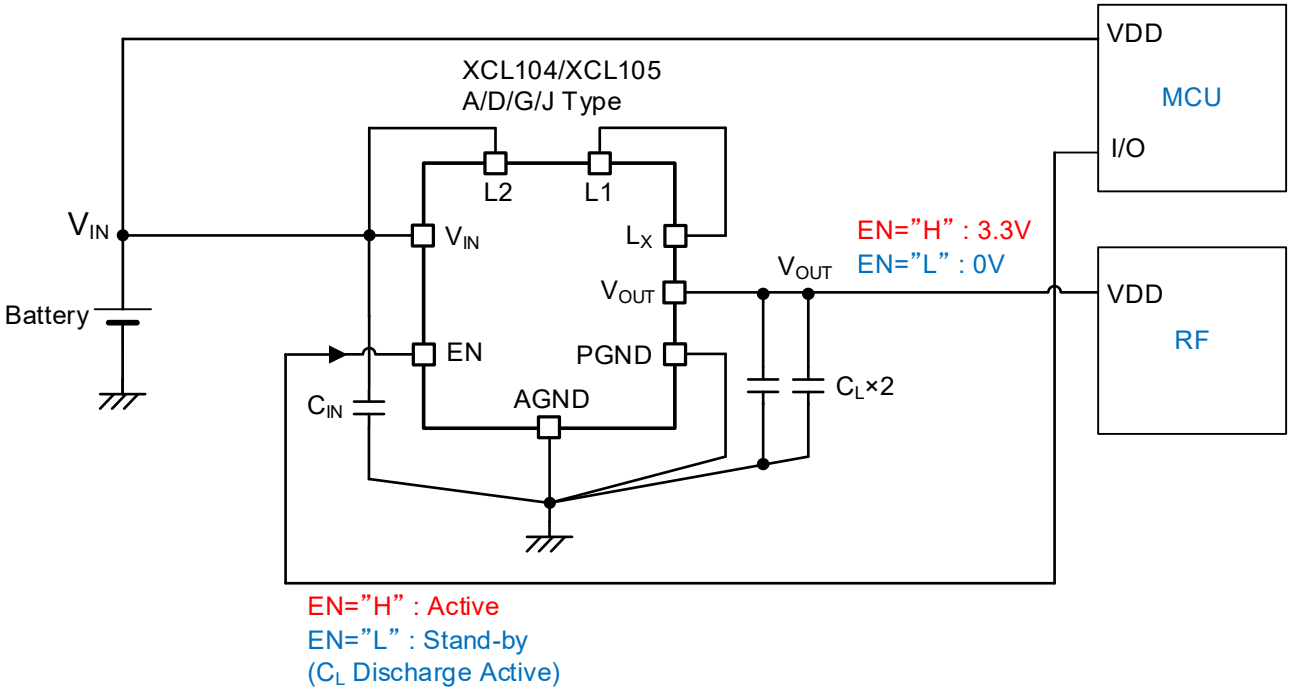
(b) For products with an integral latch, the integral latch function may operate and the output voltage may not rise to the target voltage if the current limit function continues after the start mode is completed.

■TYPICAL APPLICATION CIRCUIT/PARTS SELECTION GUIDE

＜Load disconnection function : A/D/G/J types＞

It is configured to cut off the continuity from the input side to the output side during standby mode (EN = ”L”).

For the A/D/G/J types, the C_L discharge function operates when the charge in the output capacitance is quickly discharged. In order to prevent the application from malfunction, the charge remaining in the output capacitance.

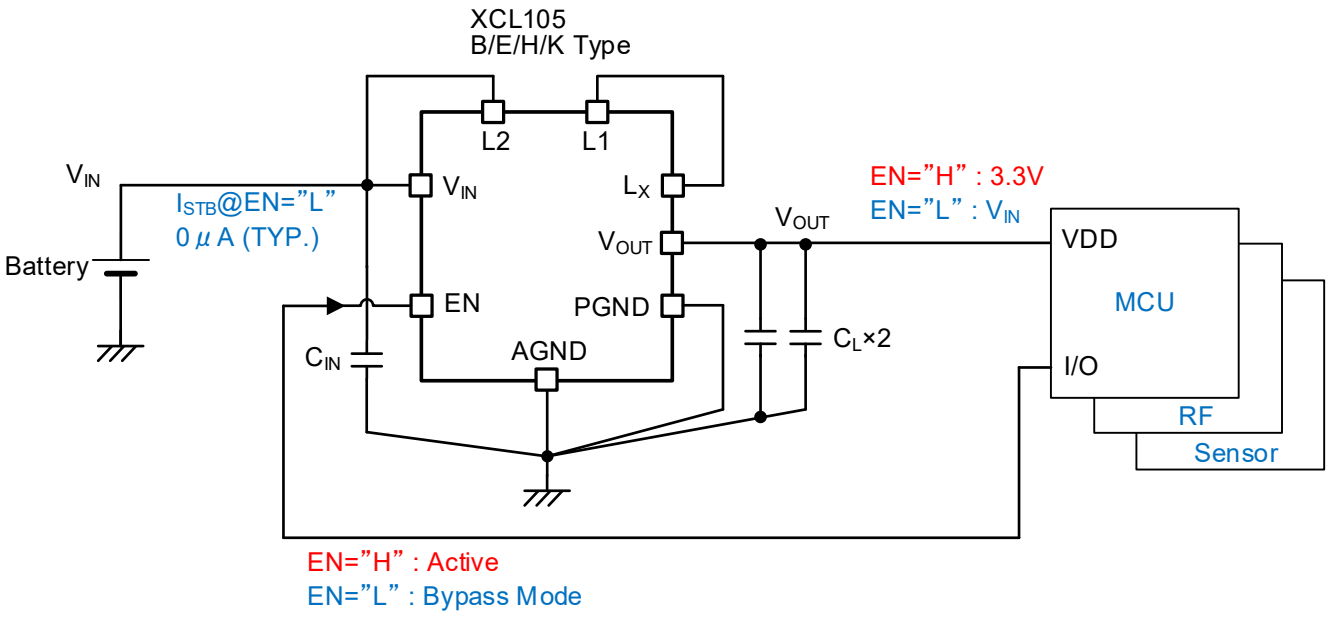


＜Bypass mode: XCL105 B/E/H/K types＞

The Pch synchronous switching FET is turned on to connect the input side and output side during the standby mode (EN = ”L”),. By operating in this bypass mode, current can be supplied to the output side even during standby mode, and it is possible to drive the subsequent devices.

In this configuration, a system that can be driven by a low voltage at the standby or sleep mode, it is set to bypass mode and the input voltage is output to the output side. Where communication or calculation that requires a high drive voltage is performed in the active mode, the system is driven by activating of the IC and performing boosting operation.

This operation can dramatically reduce the power consumption in the standby mode and improve the battery life.



■TYPICAL APPLICATION CIRCUIT/PARTS SELECTION GUIDE

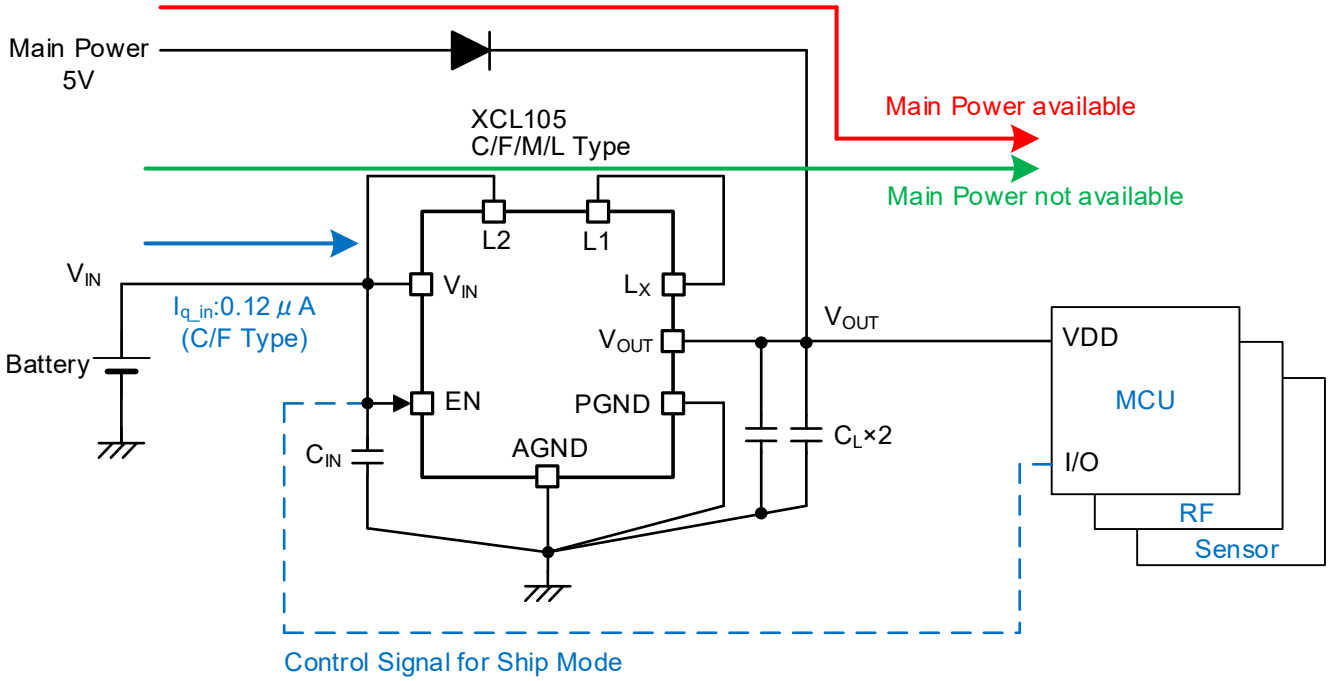
＜OR connection: XCL105 C/F/M/L types＞

The XCL105 C/F/M/L types compare the input voltage V_{IN} and output voltage V_{OUT} to optimally control the orientation of the parasitic diode of the Pch synchronous switching FET even during standby mode, so that the input side and output side do not connect through the parasitic diode of the Pch synchronous switching FET.

Even if an external voltage higher than the V_{IN} voltage is applied to the output side by controlling this parasitic diode, the input side and output side do not connect, and output OR connection is possible.

This type can be used for OR connection is possible such as backup power supply and output OR connection assuming the input of an external power supply.

Moreover, the design which suppresses the discharge current from a battery at the time of OR connection is adopted. This can suppress battery discharge during OR connection.



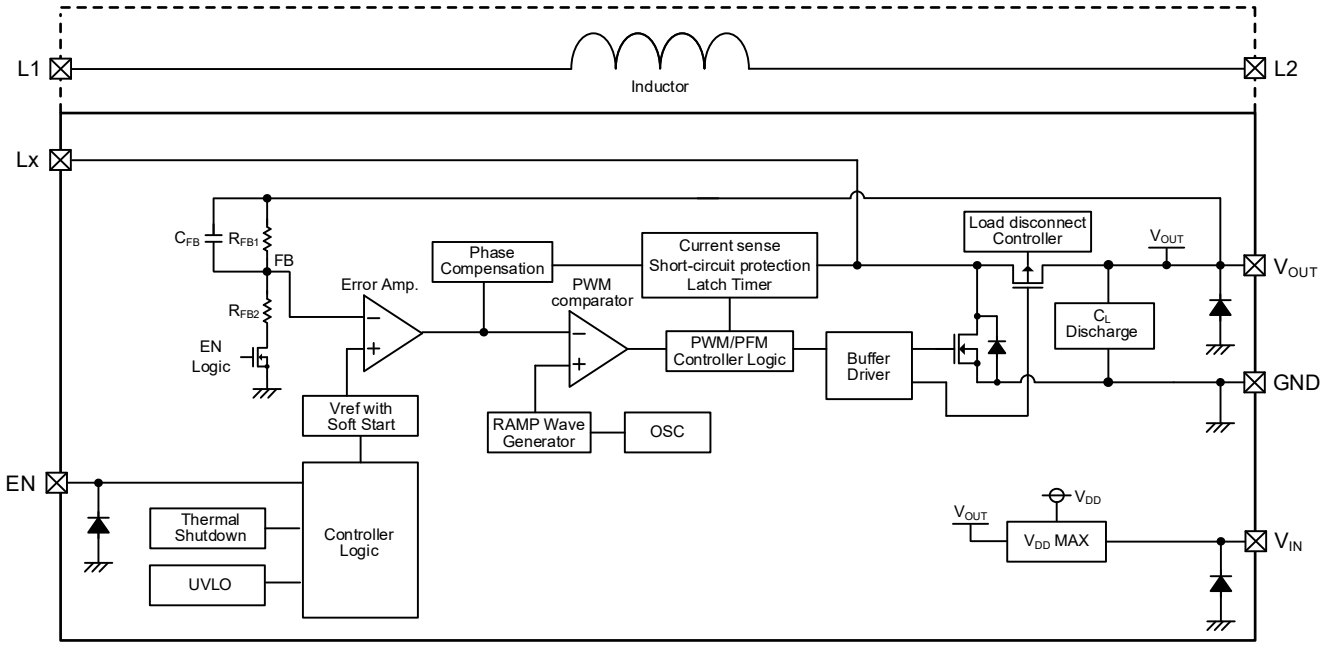
＜UVLO function: G/J/H/K/M/L types＞

G/H/M/J/K/L types have UVLO function with UVLO release voltage of 1.6V.

This UVLO function stops the IC when the battery voltage drops.

■OPERATIONAL EXPLANATION

This IC consists of a reference voltage source, ramp wave circuit, error amplifier, PWM comparator, phase compensation circuit, Nch driver FET, Pch synchronous switching FET and current limiter circuit.



XCL104/XCL105 A/D types

The main function of this IC is a current mode control step-up DC/DC converter that supports low ESR ceramic capacitors. By adopting current mode control and increasing the oscillation frequency to a high frequency, the size of peripheral parts has been reduced.

The current feedback circuit monitors the Nch driver FET's turn-on current for each switching operation, and modulates the error amplifier output signal to provide multiple feedback signals. This enables a stable feedback loop even when a low ESR capacitor, such as a ceramic capacitor is used, and the output voltage is stabilized.

Regarding to the parts required for operation, select the constants by referring to the part selection guide. If a component that is significantly different from this constant is used, proper phase compensation may not be obtained, and DC/DC may operate unstable. Also, when using a capacitance other than a ceramic capacitor, use a low ESR capacitance. If a capacitor with a high ESR is used, heat generation of the capacitor and unstable DC/DC operation may occur.

＜Driver configuration / Load disconnection control (parasitic diode control)＞

A Pch FET is built-in on the High Side and an Nch FET is built-in on the Low Side.

In general Pch FETs, there is a parasitic diode with the source as the cathode and the drain as the anode, but the Pch FETs on the High Side of the XCL104/XCL105 series control the polarity of the parasitic diode.

It is possible to disconnect the load between the input and output sides by controlling this parasitic diode during standby and prevent reverse flow from the output side to the input side when external voltage is applied from the output side.

The control of the polarity of the parasitic diode depends on the types.

＜V_{DD} MAX＞

V_{DD} MAX circuit compares the input voltage and the output voltage then it will select the higher one as the power supply for the IC.

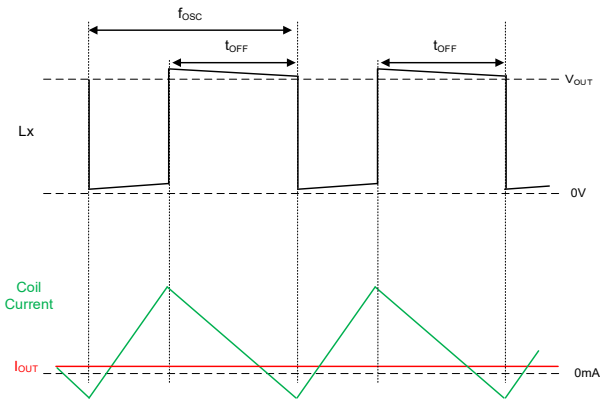
■OPERATIONAL EXPLANATION

＜Normal operation＞

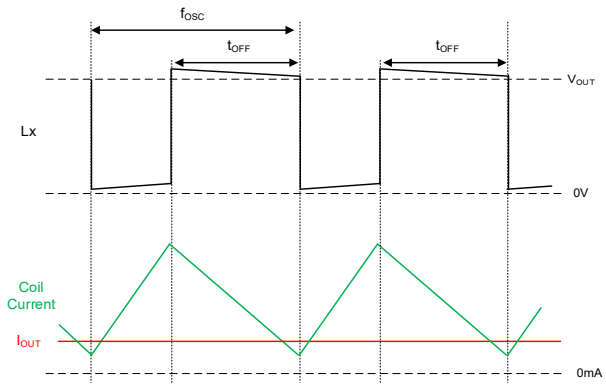
The error amplifier compares the internal reference voltage with FB voltage. In order to input a signal to the PWM comparator, the phase compensation is performed on the resulting error amplifier output. The PWM comparator compares, the signal from the error amplifier with the ramp wave from the ramp wave circuit, and delivers the resulting output to the buffer driver circuit to control the duty during PWM control. The output voltage is stabilized by performing these controls continuously.

XCL104 Series

The XCL104 Series (PWM control) performs switching at a set switching frequency f_{OSC} regardless of the output current. When the V_{OUT} voltage becomes higher than $V_{OUT(T)}$, the V_{OUT} voltage is reduced until the output voltage reaches $V_{OUT(T)}$.



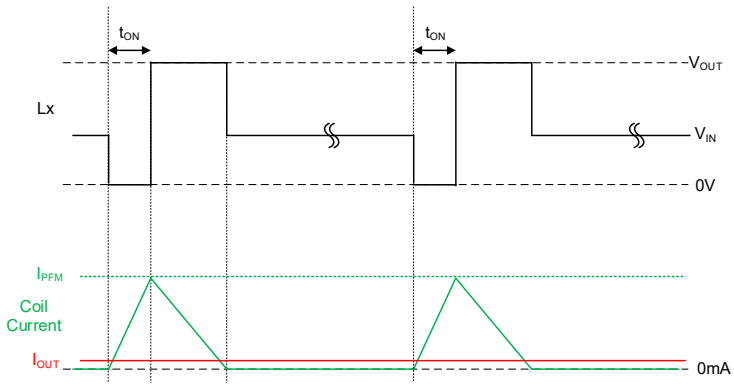
XCL104 Series : Example of light load operation



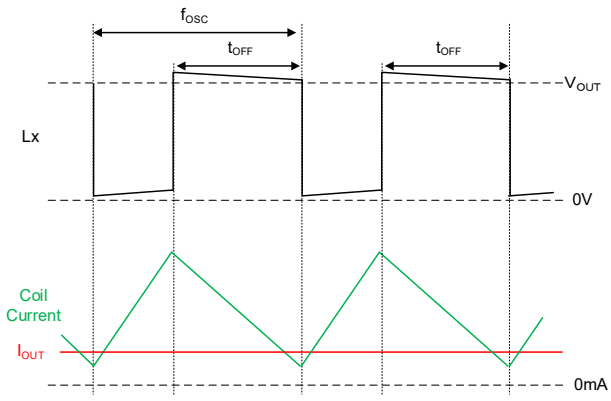
XCL104 Series : Example of heavy load operation

XCL105 Series

The XCL105 Series (PWM/PFM automatic switching control) lowers the switching frequency during light loads by turning on the Low side driver FET when the coil current reaches the PFM current (I_{PFM}). This operation reduces the loss during light loads and achieves high efficiency from light to heavy loads. As the output current increases, the switching frequency increases proportional to the output current, and when the switching frequency increases f_{OSC}, the circuit switches from PFM control to PWM control and the switching frequency becomes fixed.



XCL105 Series: Example of light load operation



XCL105 Series: Example of heavy load operation

■OPERATIONAL EXPLANATION

＜$V_{OUT(T)}$＜ V_{IN} : Input through＞

The behavior of this IC differs depending on the type when an input voltage higher than the set output voltage is applied. The details of operation for each type are as follows.

XCL105 C/F/M/L types: Load Disconnection + No CL Discharge

The XCL105 C/F/M/L types turn off the Pch synchronous switching FET when a voltage higher than the set output voltage is applied to the input voltage, and fix the polarity of the parasitic diode to cathode: V_{OUT}, anode: Lx.

Under this condition, current flows from the input side to the output side via the parasitic diode of the Pch synchronous switching FET, and the output voltage is as follows. When continuously supplying current to the output side via the parasitic diode of the Pch synchronous switching FET, the output current should be 100mA or less.

$V_{OUT(T)} \leqq V_{IN} \leqq V_{OUT(T)} + VF$: $V_{OUT} \fallingdotseq V_{OUT(T)}$
$V_{OUT(T)} + VF < V_{IN}$: $V_{OUT} \fallingdotseq V_{IN} - VF$
* VF : Parasitic diode of Pch synchronous switching FET VF

Except XCL105 C/F/M/L types

For all types except XCL105 C/F/M/L types, when the input voltage higher than the set output voltage, the Pch synchronous switching FET is turned on.

By this operation, the output voltage will be as follows.

$V_{OUT(T)} \leqq V_{IN}$: $V_{OUT} \fallingdotseq V_{IN} - I_{OUT} \times R_{LXP}$ (TYP. 0.23Ω)

■OPERATIONAL EXPLANATION

＜EN function / load disconnection function / bypass mode＞

When a "H" voltage (V_{ENH}) is input to the EN pin, the output voltage is raised by the start-up mode, and then normal operation starts.

When the "L" voltage (V_{ENL}) is input to the EN pin, the IC enters the standby mode, and the current consumption is reduced to the standby current I_{STB}.

The polarity of the parasitic diodes of the Pch synchronous switching FET and Pch synchronous switching FET in the standby mode and the operation of the C_L discharge function depending on the types.

The details of the operation for each type are as follows.

A/D/G/J types : Load disconnection function with C_L discharge function

When the Nch driver FET and Pch synchronous switching FET are turned off, the C_L discharge function operates.

When the C_L discharge function operates, the charge on the output side is quickly discharged and the output voltage is reduced.

When the Nch driver FET and Pch synchronous switching FET are turned off and fix the polarity of the parasitic diode of the Pch synchronous switching FET to anode: V_{OUT} and cathode: Lx, the conduction from the input side to the output side is cut off.

The current consumption during this operation is the standby current I_{STB} (TYP. 0.0μA).

XCL105 C/F/M/L types : Load disconnection function without C_L discharge function

Nch driver FET and Pch synchronous switching FET are turned off.

Even in standby mode, the V_{IN} voltage is compared with the V_{OUT} voltage, and the polarity of the parasitic diode for the Pch synchronous switching FET is controlled so that the input and output sides do not connect through the parasitic diode of the Pch synchronous switching FET.

Even if an external voltage higher than the V_{IN} voltage is applied to the output side by controlling this parasitic diode, the input side and the output side will not connect, and the output OR connection is possible.

The current consumption during this operation is the standby current I_{STB} (TYP. 0.16μA).

XCL105 B/E/H/K types : Bypass mode

When the Nch driver FET turned off and the Pch synchronous switching FET turned on, the resistance between the Lx and V_{OUT} becomes R_{LXP} (TYP. 0.23Ω) and connects.

This operation allows current to be supplied to the output side even in the standby mode, enabling to drive the subsequent devices.

The current consumption during this operation is the standby current I_{STB} (TYP. 0.0μA).

In standby mode (EN="L") Operation list

TYPE	Nch Driver FET / Pch Driver FET	V_{OUT} pin Voltage	C_L Discharge	I_{STB} (TYP.)	Applied Voltage to the V_{OUT} pin (EN="L")
A/D/G/J	OFF /OFF	GND	Active	0.0μA	No (C_L Discharge Operation)
C/F/M/L (Only XCL105)	OFF /OFF	OPEN	-	0.16μA	Yes
B/E/H/K (Only XCL105)	OFF /ON	V_{IN}	-	0.0μA	No (Reverse Flow toward the input)

■OPERATIONAL EXPLANATION

< Startup Mode / Soft Start >

This function gradually boosting the V_{OUT} voltage up to the set output voltage to suppress the inrush current. The start-up mode is activated when the EN pin is input to "H" and the IC is turned from standby mode to active mode.

The short circuit protection and integral latch functions of the XCL104 D/J types and XCL105 D/E/F/J/K/L types do not operate during the startup mode.

The details of the operation for each type are as follows.

XCL104/XCL105 A/D/G/J types, XCL105 C/F/M/L types : load disconnection function

① $V_{OUT} \leqq V_{IN}$

The current is supplied to the output side via Pch synchronous switching FET.

Since the Pch synchronous switching FET supplies current to the output side while the current is limited, the V_{OUT} is gradually increased to V_{IN}.

② $V_{OUT} < V_{OUT(T)} \times 0.9$

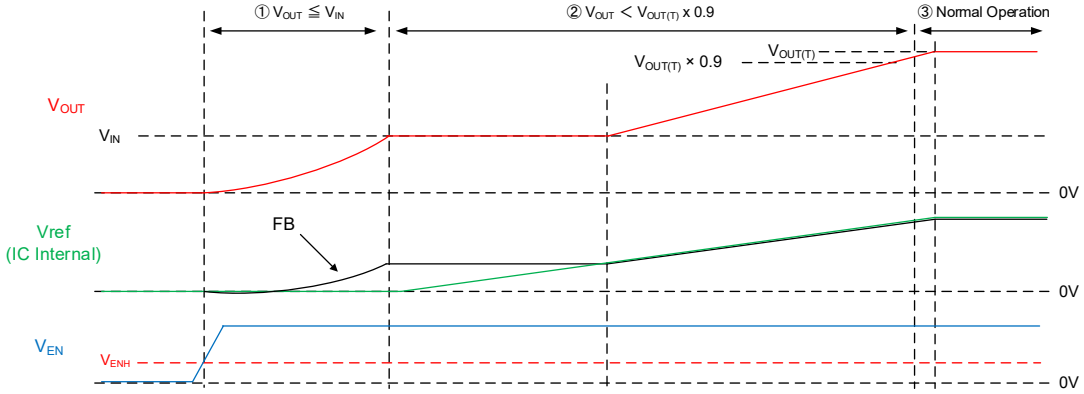
After the V_{OUT} voltage reaches to V_{IN}, the internal reference voltage of the IC is raised slowly.

When the FB voltage, which is the voltage divided by the V_{OUT} voltage with R_{FB1} and R_{FB2}, becomes lower than the internal reference voltage of the IC, the switching operation starts.

The slope of the V_{OUT} voltage rise is proportional to the slope of the internal reference voltage of the IC.

③ Normal operation

When the V_{OUT} voltage reaches $V_{OUT(T)} \times 0.9$, the start-up mode is terminated, and the device shifts to normal operation. However, under the condition of heavy load and large output capacitance, it may not be able to rise to the set output voltage within the start-up period of the reference voltage. In this case, even if the set output voltage is not reached, the IC will shift from start-up mode to normal operation after the completion of the start-up of the reference voltage.



XCL105 B/E/H/K types : Bypass mode

① $V_{OUT} < V_{OUT(T)} \times 0.9$

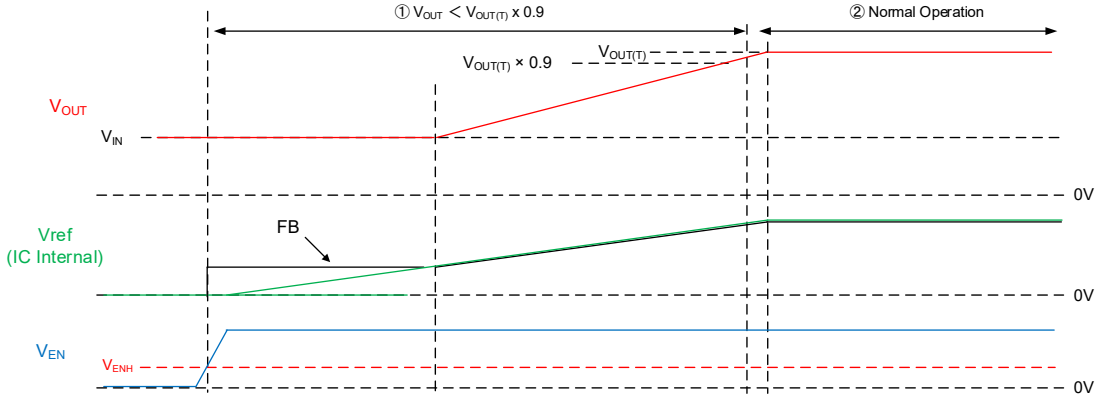
After becoming active, the internal reference voltage of the IC is raised slowly.

When the FB voltage, which is the voltage divided by the V_{OUT} voltage with R_{FB1} and R_{FB2}, becomes lower than the internal reference voltage of the IC, the switching operation starts, and the output voltage is increased from V_{IN}.

The slope of the V_{OUT} voltage rise is proportional to the slope of the internal reference voltage of the IC.

② Normal operation

When the V_{OUT} voltage reaches $V_{OUT(T)} \times 0.9$, the start-up mode is terminated, and the device shifts to normal operation. However, under the condition of heavy load and large output capacitance, it may not be able to rise to the set output voltage within the start-up period of the reference voltage. In this case, even if the set output voltage is not reached, the IC will shift from start-up mode to normal operation after the completion of the start-up of the reference voltage.



■OPERATIONAL EXPLANATION

＜Current Limit / Short Circuit Protection / Integral Latch＞

The current limit function of this IC monitors the current flowing in the Nch driver (=coil current) for each switching cycle, and when the current flowing through the Nch driver FET reached the current limit value I_{LIM} (TYP. 2.42A @ $V_{OUT\,(T)}$=5.0V), it will be in the overcurrent detection state.

When the overcurrent detection state occurs, the Nch driver FET is turned off and the detection state is maintained during this switching cycle. If the current flowing to the Nch driver FET is less than the current limit value I_{LIM} in the next switching cycle, the overcurrent detection state is released.

If the overcurrent detection state is continued or if there is a significant drop in output voltage, the short circuit protection function and integral latch function are activated depending on the type.

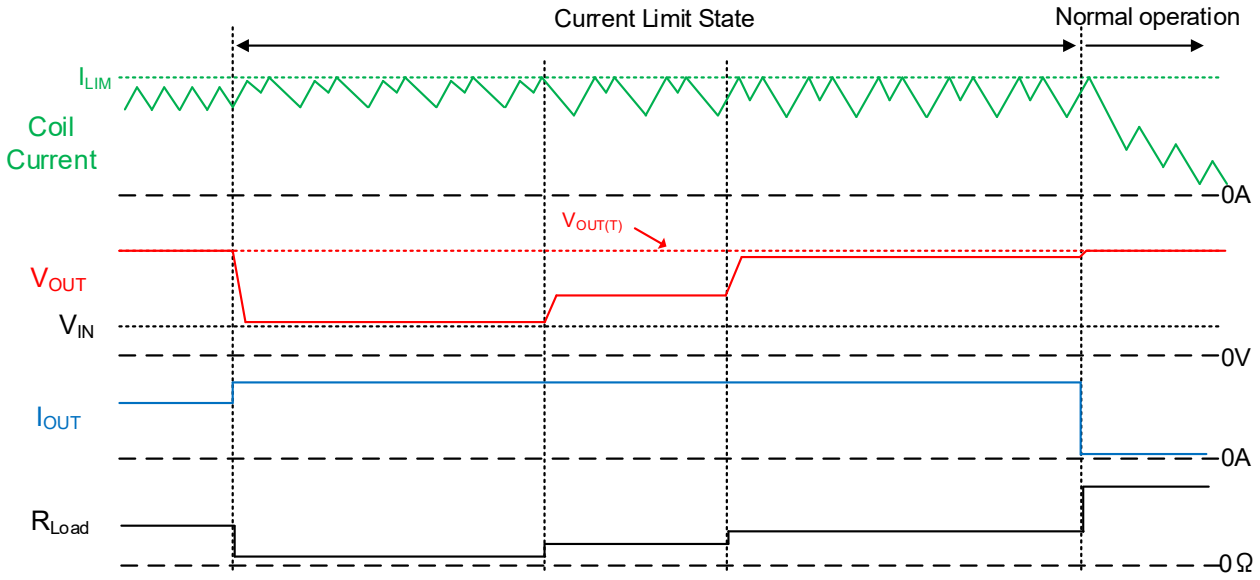
The details of the operation for each type are as follows.

No short circuit protection/integral latch: XCL104 A/G types, XCL105 A/B/C/G/H/M types

① If the current flowing in the Nch driver FET reaches the current limit value I_{LIM}, it will be in the overcurrent detection state. The Nch driver FET turns off and remains off during this switching cycle.

② In the next switching cycle, the Nch driver FET turns on.
If the overcurrent state continues and the current flowing to the Nch driver FET reaches the current limit value I_{LIM}, the overcurrent detection state is maintained.

② If overcurrent state continues, ① and ② are repeated.



＜Current Limit / Short Circuit Protection / Integral Latch (Continued)＞

Short circuit protection/with integral latch : XCL104 D/J types, XCL105 D/E/F/J/K/L types

In the XCL104 D/J types and XCL105 D/E/F/J/K/L types, if the overcurrent detection state continues and the output voltage drops significantly, the driver FETs are turned off and latch stopped by the operations shown in (a) and (b).

Case (a) : When the overcurrent detection status is maintained

① When the current flowing to the Nch driver FET reaches the current limit value I_{LIM}, the overcurrent detection state occurs. The Nch driver FET is turned off and kept off during this switching cycle.
When the XCL104 D/J types and XCL105 D/E/F/J/K/L types become to the overcurrent detection status, the integral latch timer starts counting.

② In the next switching cycle, the Nch driver FET turns on.
If the over-current state continues and the current flowing to Nch driver FET reaches the current limit I_{LIM}, the over current detection state is maintained.

③ When the overcurrent detection state is maintained and the integral latch timer continues to count t_{LAT} (TYP. : 200μs), the Nch driver FET and Pch synchronous switching FET are turned off and the integral latch function latches.
However, for XCL104 D type and XCL105 D/E/F types, the integral latch function does not operate when the input voltage is less than the latch release voltage V_{LAT_R}(TYP. 1.2V).

Case (b) : When the output voltage drops significantly

① When the current flowing to Nch driver FET reaches the current limit value I_{LIM}, the overcurrent detection state occurs. The Nch driver FET is turned off and kept off during this switching cycle.

② In the next switching cycle, the Nch driver FET turns on.
If the over-current state continues and the current flowing to Nch driver FET reaches the current limit I_{LIM}, the over-current detection state is maintained.

③ If the output voltage becomes equal or less than the short circuit protection threshold voltage V_{SHORT}(TYP. V_{IN}) during the over current detection state, the Nch driver FET and Pch synchronous switching FET are turned off and the short circuit protection function operates and latches.
However, for XCL104 D type and XCL105 D/E/F types, the short circuit protection function does not operate when the input voltage is equal to or less than the latch release voltage V_{LAT_R}(TYP. 1.2V).

■Conditions for recovery from latch stop

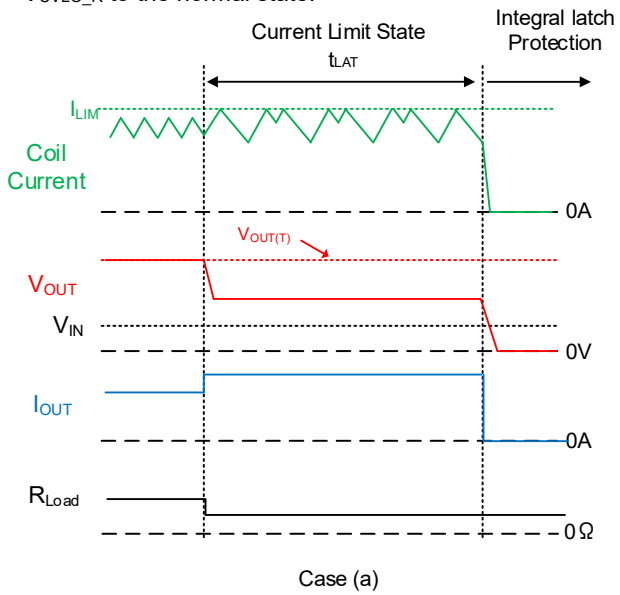
There are two conditions for recovery from latch stop by the current limited integral latch timer and short circuit protection. In addition, the recovery from the latch stop raises the output voltage via the start-up mode and shifts to normal operation.

Without UVLO function : XCL104 D type, XC105 D/E/F types

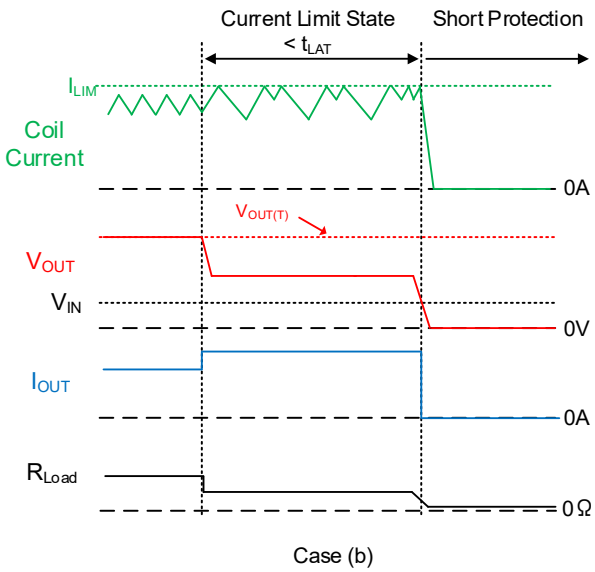
- Input the "L" voltage to the EN pin to put it in the standby mode and then put it in the active mode.
- Set the input voltage V_{IN} below the latch release voltage V_{LAT_R}(TYP. 1.2V).

With UVLO function : XCL104 J type, XCL105 J/K/L types

- Input the "L" voltage to the EN pin to put it in the standby mode and then put it in the active mode.
- After setting the input voltage to V_{UVLO_R}-V_{UVLO_HYS} or less and setting the UVLO detection state, apply the voltage above V_{UVLO_R} to the normal state.



Case (a)



Case (b)

■OPERATIONAL EXPLANATION

＜Thermal shutdown＞

The junction temperature is monitored to protect the IC from thermal destruction.

When the junction temperature reaches the thermal shutdown detection temperature T_{TSD} (TYP. 150°C), the thermal shutdown activated, and the Nch driver FET and Pch synchronous switching FET are turned off, and the output voltage drops. When the chip temperature drops to the thermal shutdown release temperature T_{TSD}-T_{HYS} (TYP. 125°C) by stopping the current supply, the output voltage is turned on by the start-up mode, and then normal operation starts.

In order to suppress the current consumption at the light load, XCL105 series stops the thermal shutdown function when the output current is small at the PFM control.

＜UVLO＞

XCL104 G/J types and XCL105 G/H/M/J/K/L types have UVLO function.

If V_{IN} voltage becomes equal or less than V_{UVLO_R} (TYP.1.60V)- V_{UVLO_HYS} (TYP.0.15V), UVLO Detect Delay: t_{DF} (TYP. : 200μs) continues, then UVLO becomes active.

When UVLO detection state is reached, the switching operation is stopped and Nch driver FET and Pch synchronous switching FET are turned off.

If V_{IN} voltage is higher than V_{UVLO_R}, the output voltage is raised by the start-up mode, and then normal operation is performed.

The consumption current of the products with UVLO function is slightly higher than the products without UVLO function due to the operation of UVLO function

＜C_L Discharge＞

A/D/G/J types can discharge the electric charge at the output capacitor (C_L) quickly during standby mode(EN="L") via the Nch FET located between V_{OUT} and GND.

Electric charge at the output capacitor (C_L) is quickly discharged so that it may avoid application malfunction during standby mode.

Discharge time of the output capacitor (C_L) is set by the C_L discharge resistance (R_{DCHG}) and the output capacitor (C_L).

However, the C_L discharge resistance [R_{DCHG}] is depends on the V_{IN} or V_{OUT}. We recommend that you fully check actual performance.

$$V = V_{OUT(T)} \times e^{-t/\tau}$$
$$t = \tau \times \ln (V_{OUT(T)} / V)$$

V : Output voltage after discharge
$V_{OUT(T)}$: Target voltage
t : Discharge time
τ : $C_L \times R_{DCHG}$
C_L : Capacitance of Output capacitor (C_L)
R_{DCHG} : C_L Discharge resistance, it depends on the V_{IN} or V_{OUT}

■NOTES ON USE

1) For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications. Also, if used under out of the recommended operating range, the IC may not operate normally or may cause deterioration.

2) Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the coil inductance, capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.

3) The DC/DC converter performance is greatly influenced by not only the ICs' characteristics, but also by those of the external components. Care must be taken when selecting the external components. Especially for capacitor, it is strongly recommended to use an appropriate capacitor according to the DC bias characteristics and temperature characteristics so that the effective capacitance value is equal to or greater than the recommended components under the actual usage conditions.

4) When the EN pin is open, the IC will operate indefinitely. Therefore, the EN pin should not be open and should be set to a fixed voltage. To prevent the IC and peripheral devices from malfunctioning due to pin-to-pin shorts, or to prevent the IC from being damaged by external noise, etc., it is recommended that a resistor of 1MΩ or less be connected to the EN pin instead of connecting it directly to the V_{IN}.

5) When the boost ratio is small, PWM control oscillates intermittently.
This may cause the switching frequency to drop below f_{OSC} or increase output voltage ripple.
To suppress the ripple voltage, increase the capacitance value of the output capacitor and take measures

6) When connecting an external power supply to the output side, please use the XCL105 C/F/M/ L types.
When using the XCL105 C/F/M/L type exclusion, depending on the bias conditions, the IC may break down and reverse flow to the input side may occur.

7) Depending on the detection delay time of the current limit circuit, a coil current exceeding the limit current value I_{LIM} may flow.

8) Under the following conditions, the current limit function may not operate.
XCL104 D/J types, XCL105 D/E/F/J/K/L types are used the integral latch method. In this case, the integral latch of the current limit function and the latch stop by the short circuit protection function do not operate in these types

The boost ratio is small
When the boost ratio is small, the required duty is low and the on-time of the Nch driver FET on the low side is short.
If this on-time is shorter than the detection delay of the current limit circuit, the current limit function may not operate.

The boost ratio is high
When the boost ratio is high, the coil current may be limited below the current limit value due to the maximum duty ratio, on-resistance, and DCR of the coil, and the current limit function may not operate.

9) The current limit function is a function that limits the current flowing through the Nch driver FET, and does not limit the current flowing through the Pch synchronous switching FET.
Therefore, an overcurrent may flow in the parasitic diode of the Pch synchronous switching FET and the Pch synchronous switching FET, and the IC may be destroyed.

10) XCL104 D/J types, XCL105 D/E/F/J/K/L types have short-circuit protection and integral latch function. If the output voltage drops sharply due to an output short circuit, etc. The internal power supply of the IC may drop sharply by the circuit delay of the V_{DD} MAX circuit. As a result, the latch state of the short-circuit protection function may be reset and the latch stop may not be maintained.

■NOTES ON USE

11) If a large capacitor is used for the output capacitance or if a heavy load is pulled during startup mode, the follow operations may occur.

With short circuit protection/integral latch : XCL104 D/J types, XCL105 D/E/F/J/K/L types

For the products with integral latch, after the start-up mode is completed, the integral latch function may not operate, and the output voltage may not rise to the set output voltage due to the continuation of the current limit function.

Without short circuit protection/integral latch : XCL104 A/G types, XCL105 A/B/C/G/H/M types

The output voltage may not rise to the set output voltage during start-up mode.

After the start-up mode is completed, the output voltage rises up to the set output voltage while the current limit function is operating, so overshooting may occur in the output voltage.

12) When the input voltage is higher than the set output voltage, the XCL105C/F/M/L types turn off the Pch synchronous switching FET and fix the parasitic diode polarity to cathode: V_{OUT} and anode: Lx, when a voltage higher than the set output voltage is applied to the input voltage.

Under these conditions, when the output current is applied, the current flows through the parasitic diode of the Pch synchronous switching FET.

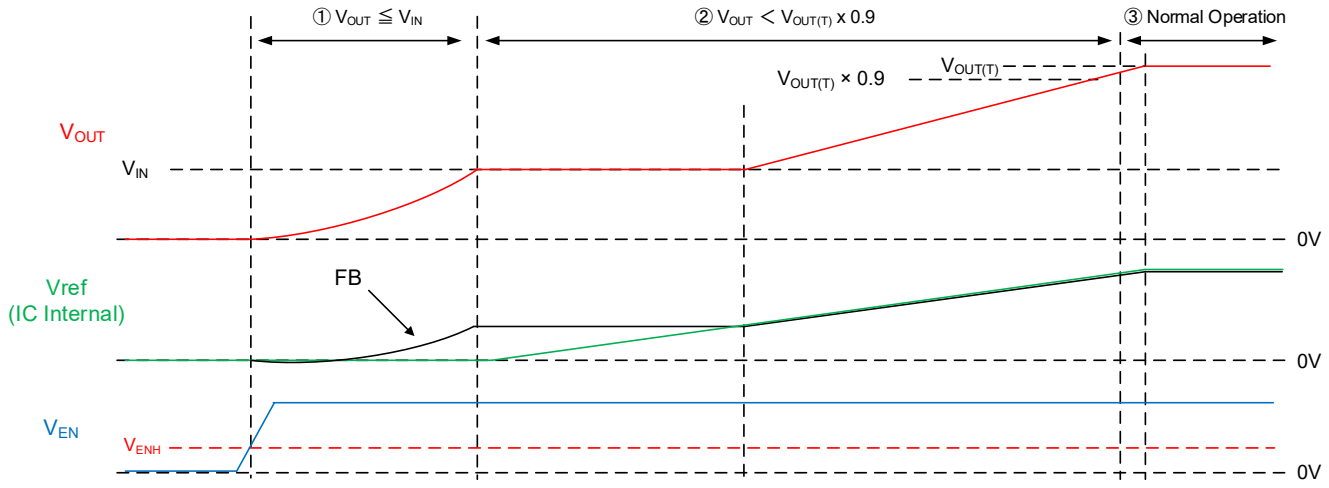
Continuously applying an output current of 100mA or more or momentarily applying excessive output current may cause IC deterioration.

If the input voltage is higher than the set output voltage, or if you want the output current to input more than 100mA continuously, we recommend using the types of XCL105C/F/M/L exclusion.

13) The XCL105 C/F/M/L types fix the parasitic diode polarity of the Pch synchronous switching FET to cathode: V_{OUT} and anode: Lx during the period of " $V_{OUT} < V_{OUT(T)} \times 0.9$" in the startup mode.

If a current of 100mA or more is applied to the parasitic diode of the Pch synchronous switching FET during this period, the output voltage may not rise to the set output voltage.

When the XCL105 C/F/M/L types are operate in the start-up mode, do not apply output current until the output voltage becomes higher than the input voltage and the switching operation starts.



14) This IC is a Inductor Built-in product, do not place it in an environment with a strong magnetic field such as near a magnet. The influence of a strong magnetic field may cause a decrease in inductance value, deterioration of efficiency, and abnormal operation of the IC.

15) Torex places an importance on improving our products and their reliability. We request that users incorporate fail safe designs and post aging protection treatment when using Torex products in their systems.

■NOTES ON USE

●Instructions of pattern layouts.

Especially noted in the pattern layout are as follows.
Please refer to the reference pattern layout on the following.

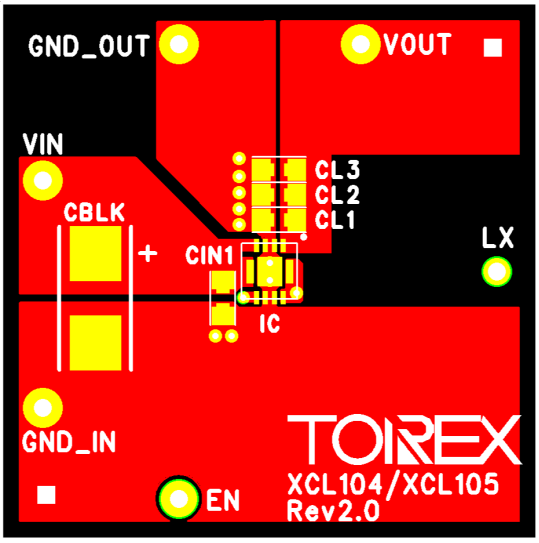
(a) Wire the large current line using thick, short connecting traces.
This makes it possible to reduce the wire impedance, which is expected to reduce noise and improve heat dissipation.
If the wire impedance of the large current line is large, it may cause noise or the IC to not operate normally.
Especially when the noise is large, the current limit function and the integral latch function may not work.

(b) Place the input capacitance C_{IN}, output capacitance C_L, inductor L and IC which the large current flows on the same surface. If they are placed on both sides, a large current will flow through Via, which has high impedance, it may cause noise and the IC may not operate normally.

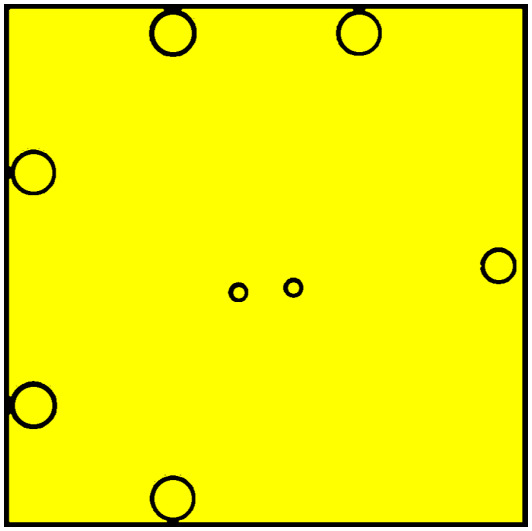
(c) Please mount each external component as close to the IC as possible.
Especially place the output capacitance C_L near the IC and connect it with as low impedance as possible.
If the output capacity C_L and IC are too far apart, it may cause noise or the IC may not operate normally

＜The reference pattern layout＞

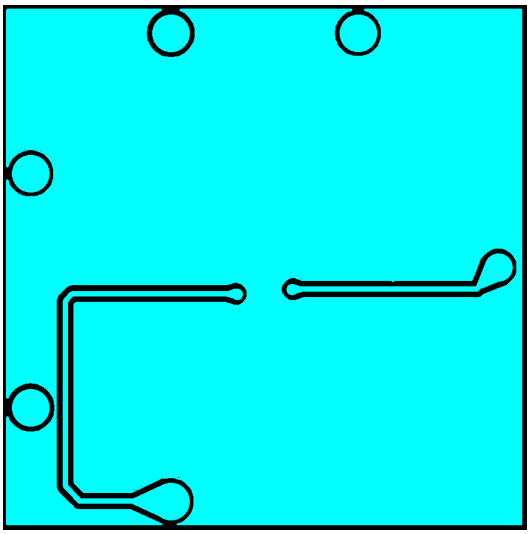
Layer 1



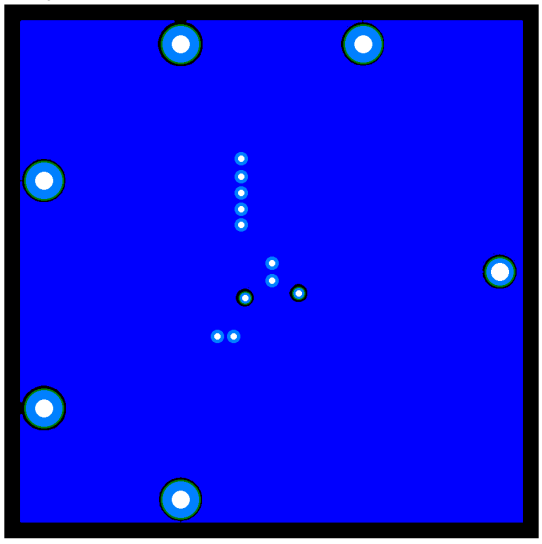
Layer 2



Layer 3



Layer 4



■Notes on handling of product

(1) The coil mounted on this product complies with the general surface mount type chip inductor specifications, and may have scratches, flux stains, etc.

(2) Do not use this product in the following environments. Places exposed to water or salt water, places where condensation occurs, places where toxic gases (hydrogen sulfide, zinc acid, chlorine, ammonia, etc.) are present.

(3) Please do not wash this product with solvent.

■ABOUT IMPLEMENTATION

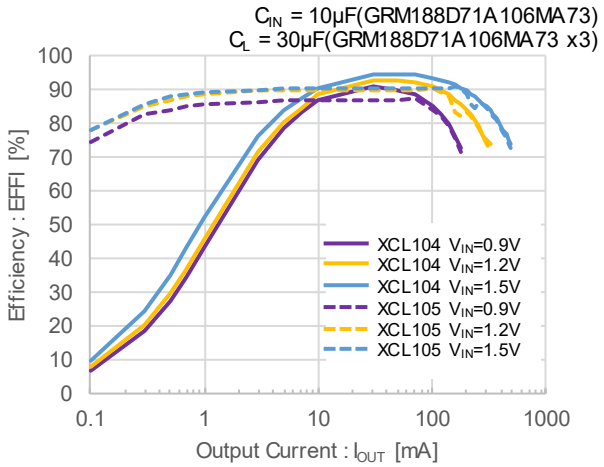
(1) This product is only suitable for reflow soldering (it is not suitable for flow soldering).

(2) This product uses solder to mount the coil on top of the package. This is no problem for regular circuit board mounted reflow, but if excessive impact is applied during reflow, the mounted coil could be moved out of position or the coil could fall off. Be careful not to strike the circuit board during circuit board mounting reflow.

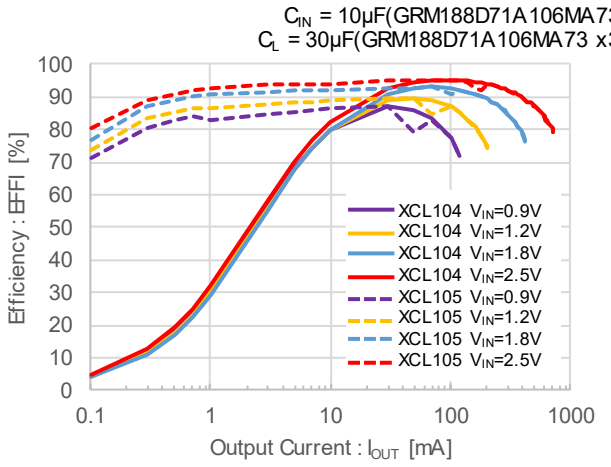
■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Efficiency vs. Output Current

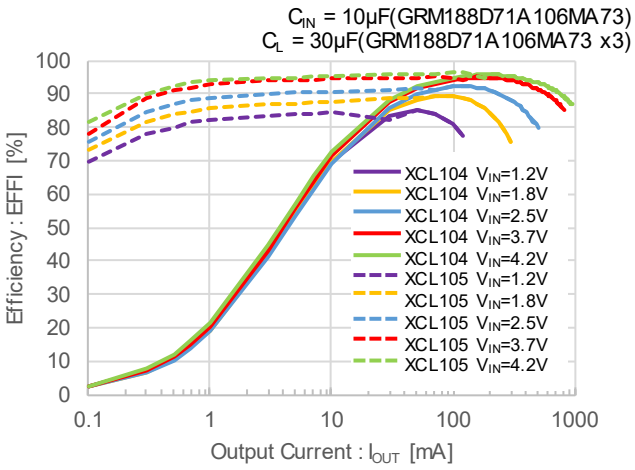
$V_{OUT(T)}$=1.8V



$V_{OUT(T)}$=3.3V



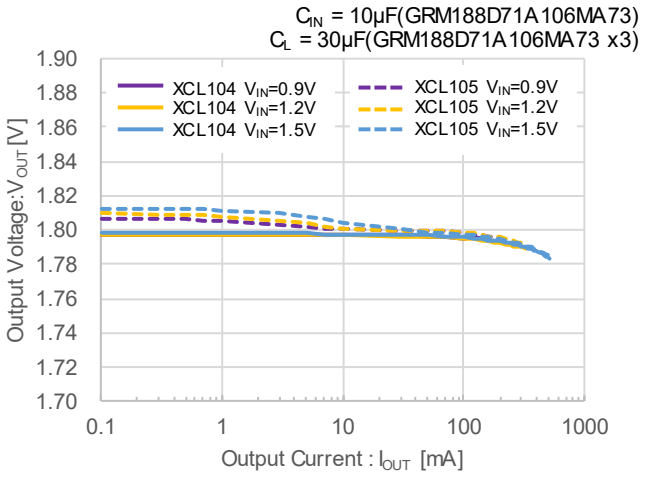
$V_{OUT(T)}$=5.0V



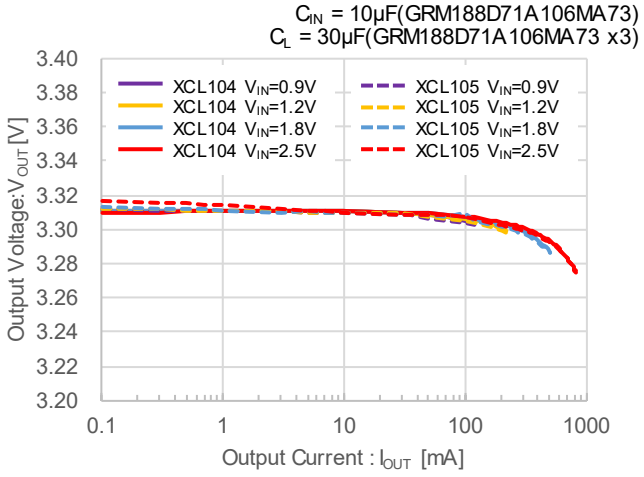
■TYPICAL PERFORMANCE CHARACTERISTICS

(2) Output Voltage vs. Output Current

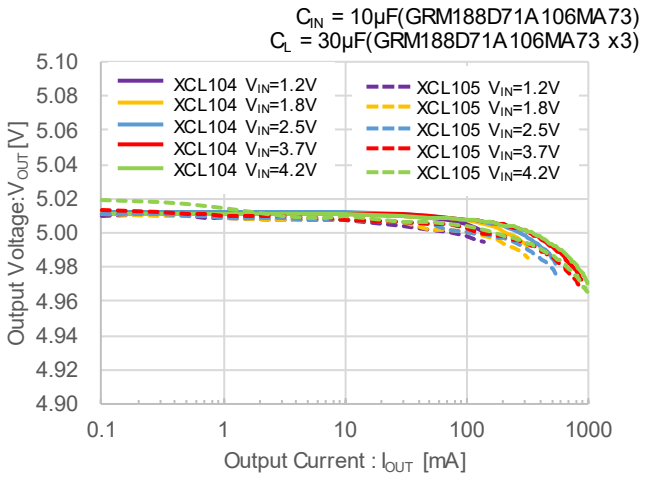
$V_{OUT(T)}$=1.8V



$V_{OUT(T)}$=3.3V

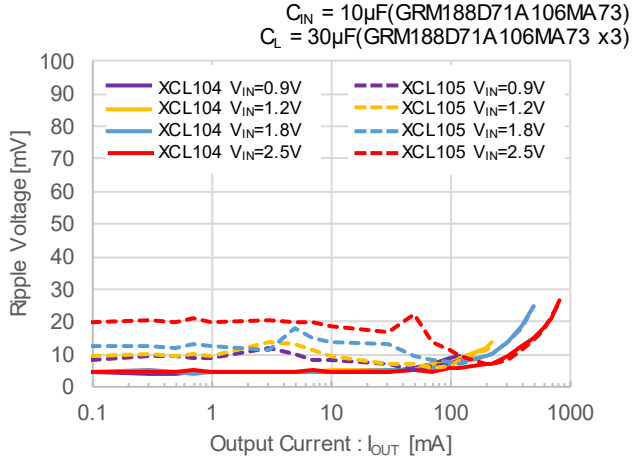


$V_{OUT(T)}$=5.0V

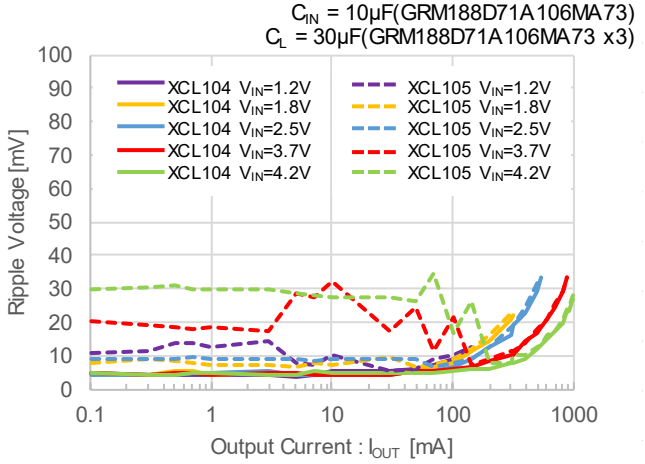


(3) Ripple Voltage vs. Output Current

$V_{OUT(T)}$=3.3V



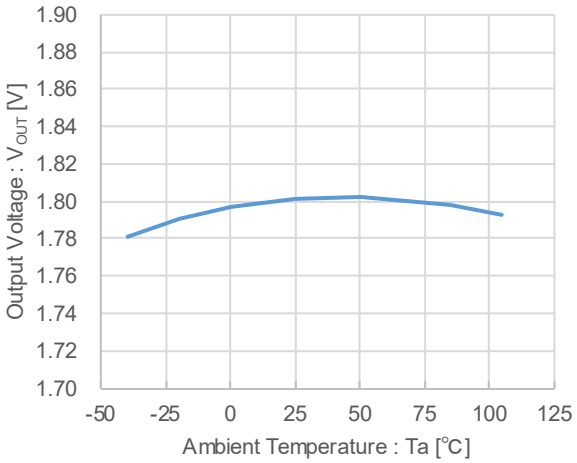
$V_{OUT(T)}$=5.0V



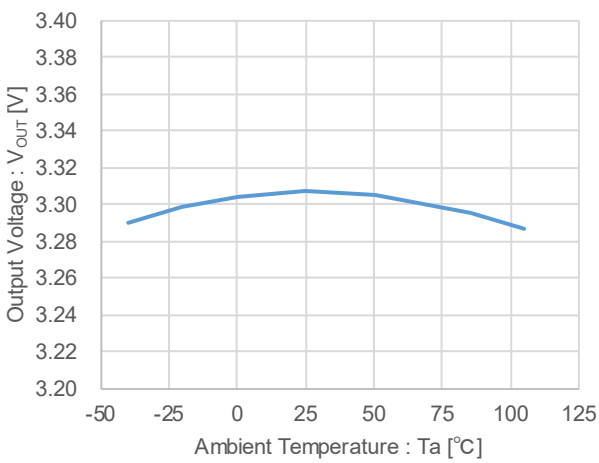
■TYPICAL PERFORMANCE CHARACTERISTICS

(4) Output Voltage vs. Ambient Temperature

$V_{OUT(T)}$=1.8V

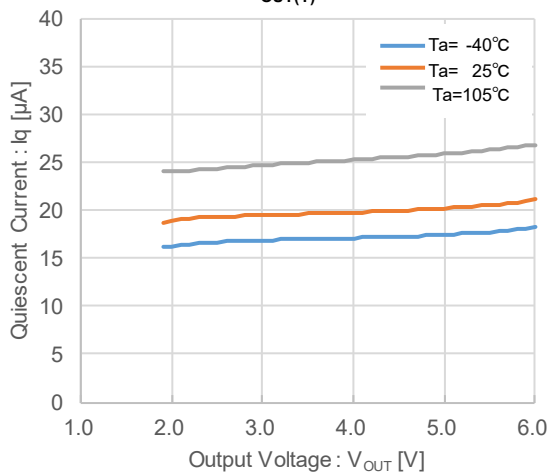


$V_{OUT(T)}$=3.3V



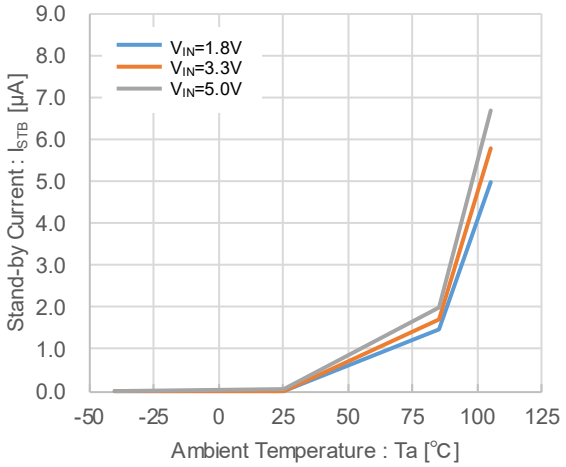
(5) Quiescent Current vs. Output Voltage

$V_{OUT(T)}$=1.8V

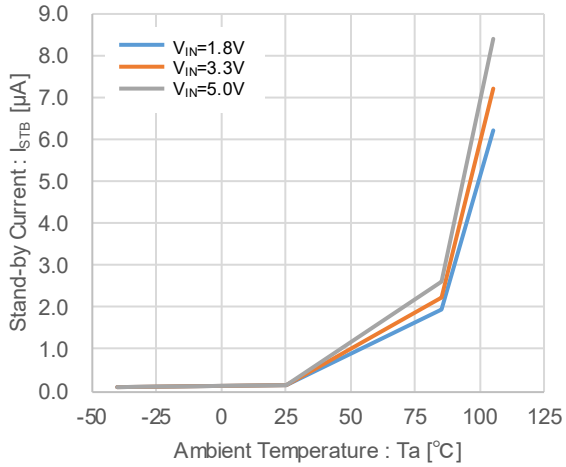


(6) Stand-by Current vs. Ambient Temperature

A/B/D/E/G/H/J/K Type



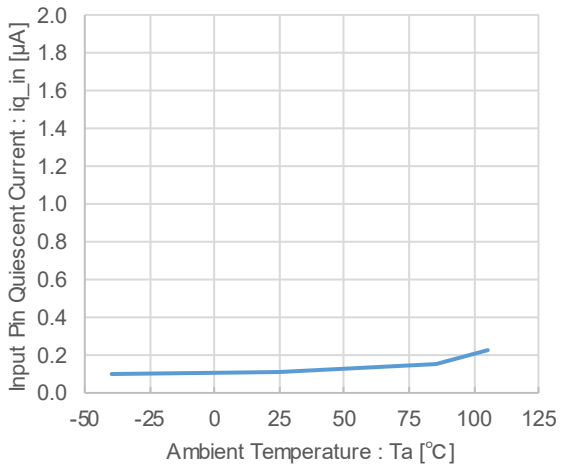
C/F/M/L Type



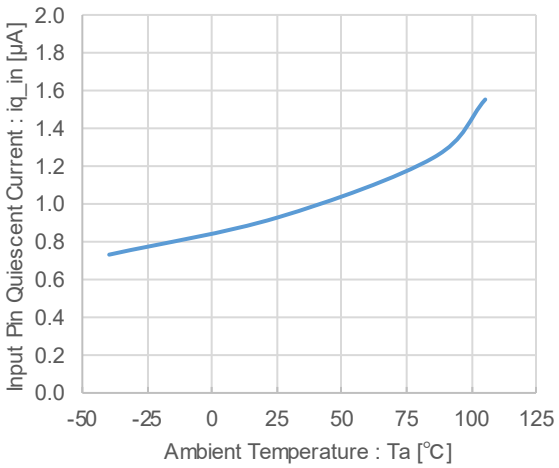
■TYPICAL PERFORMANCE CHARACTERISTICS

(7) Input Pin Quiescent Current vs. Ambient Temperature

XCL105C/F Type , $V_{OUT(T)}$=3.6V

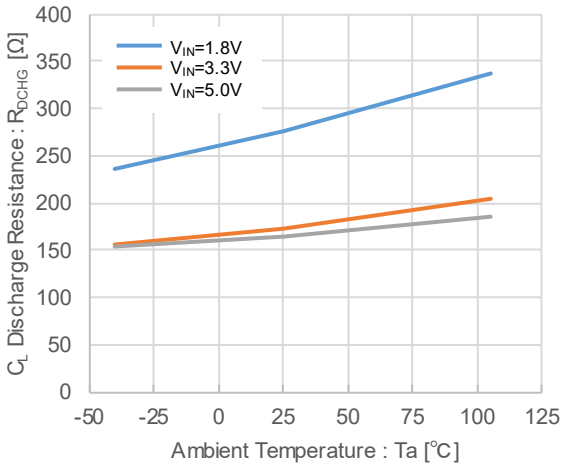


XCL105M/L Type , $V_{OUT(T)}$=3.6V



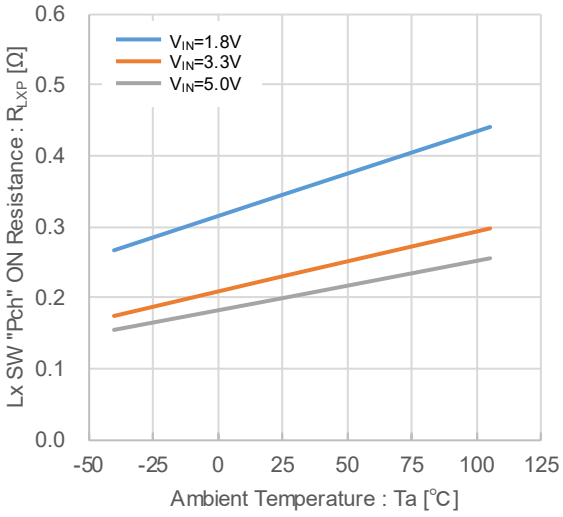
(8) C_L Discharge Resistance vs. Ambient Temperature

A/D/G/J Type

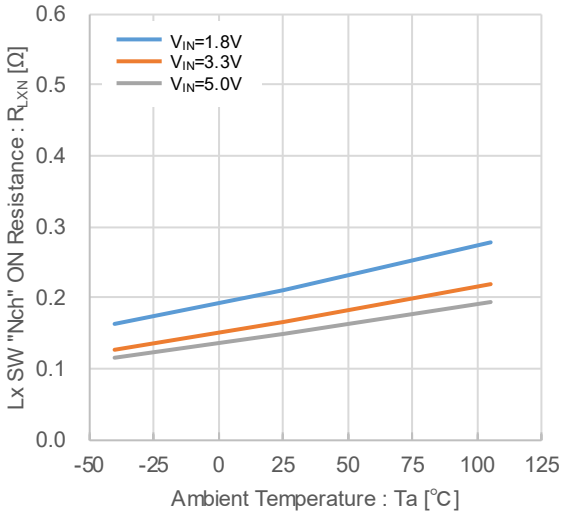


■TYPICAL PERFORMANCE CHARACTERISTICS

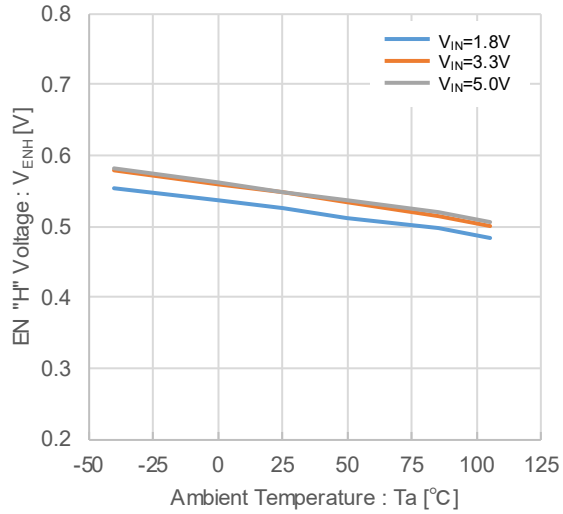
(9) Lx SW "Pch" ON Resistance vs. Ambient Temperature



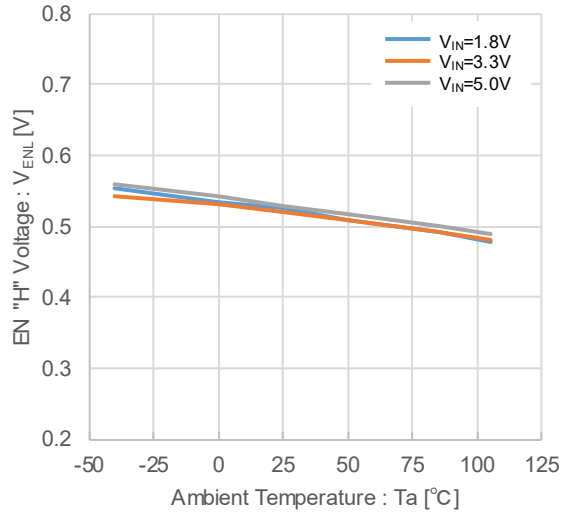
(10) Lx SW "Nch" ON Resistance vs. Ambient Temperature



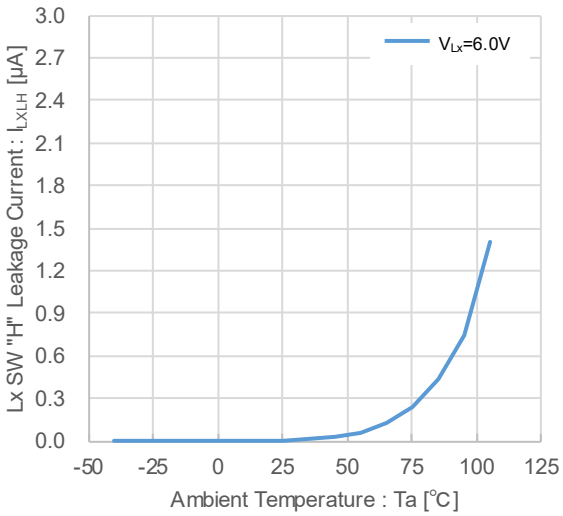
(11) EN "H" Voltage vs. Ambient Temperature



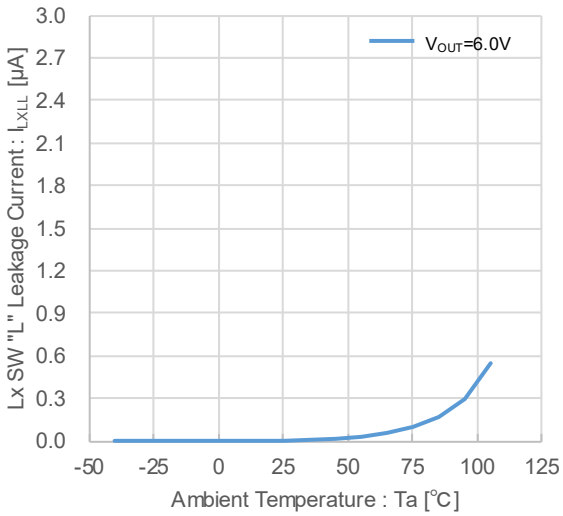
(12) EN "L" Voltage vs. Ambient Temperature



(13) Lx SW "H" Leakage Current vs. Ambient Temperature

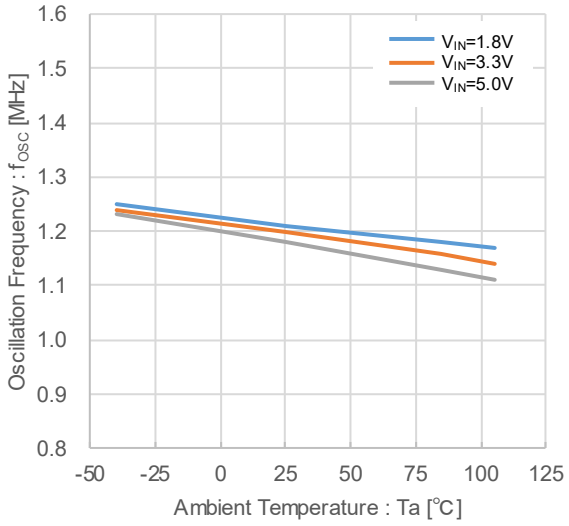


(14) Lx SW "L" Leakage Current vs. Ambient Temperature

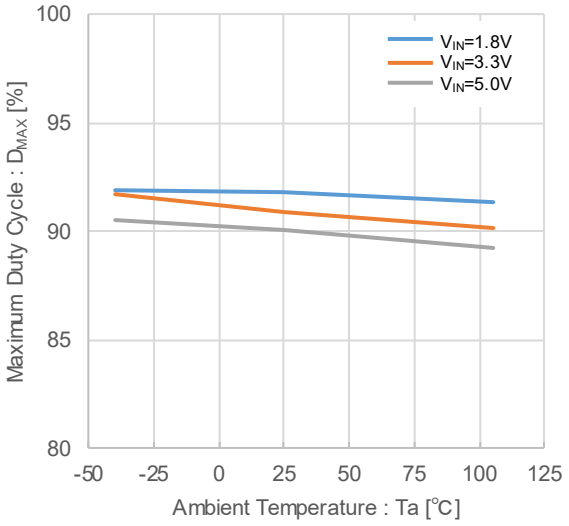


■TYPICAL PERFORMANCE CHARACTERISTICS

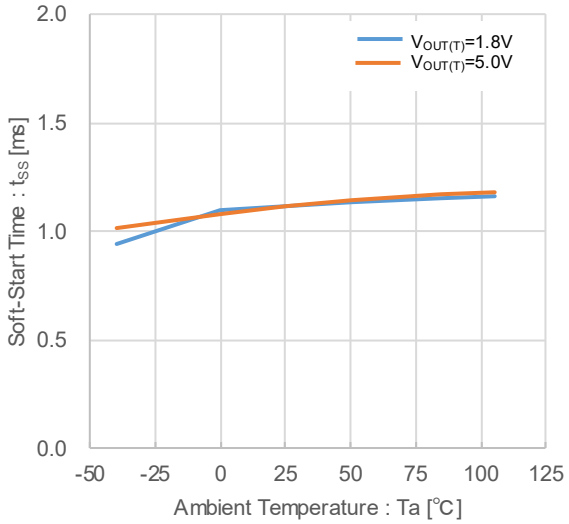
(15) Oscillation Frequency vs. Ambient Temperature



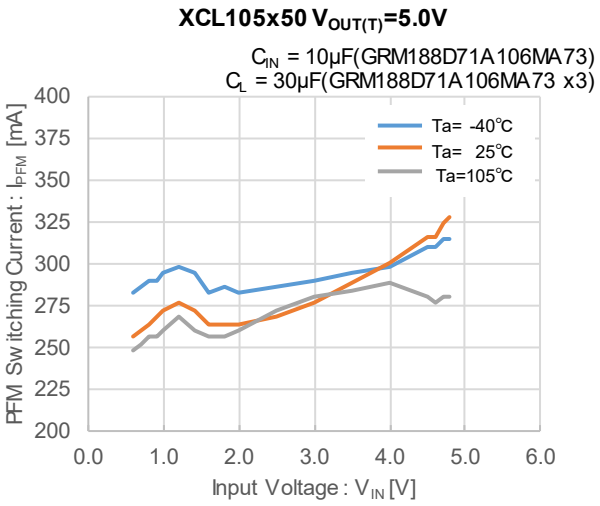
(16) Maximum Duty Cycle vs. Ambient Temperature



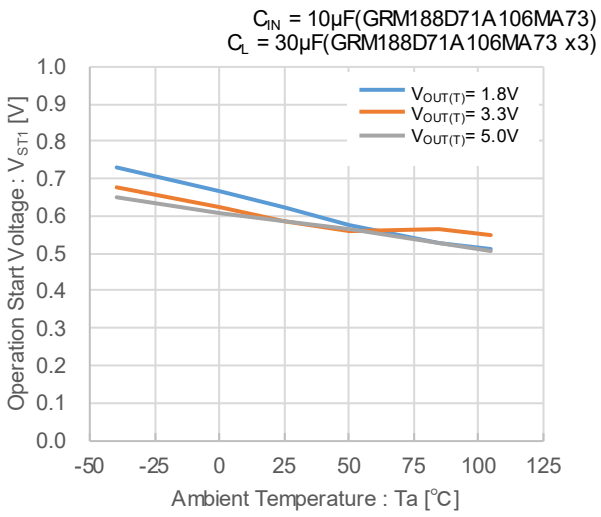
(17) Soft-Start Time vs. Ambient Temperature



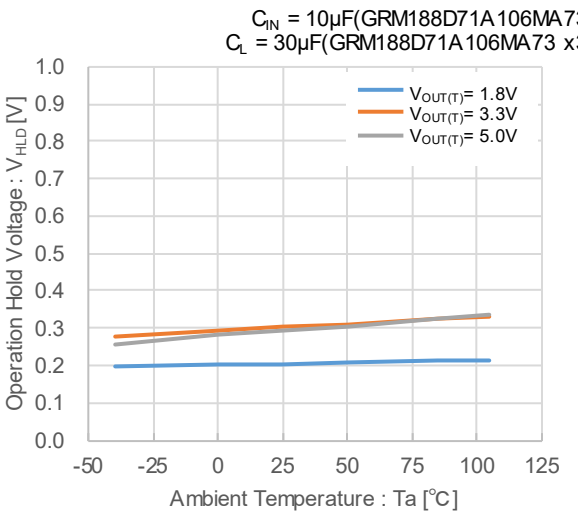
(18) PFM Switching Current vs. Input Voltage



(19) Operation Start Voltage vs. Ambient Temperature

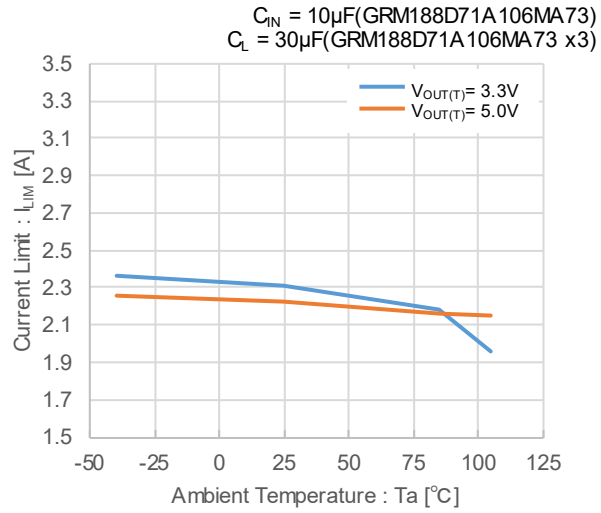


(20) Operation Hold Voltage vs. Ambient Temperature

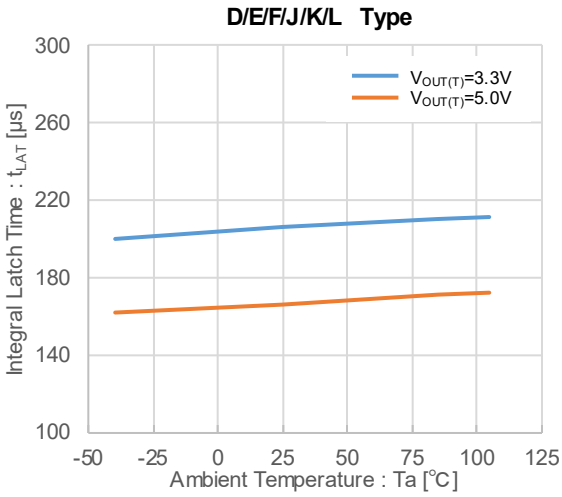


■TYPICAL PERFORMANCE CHARACTERISTICS

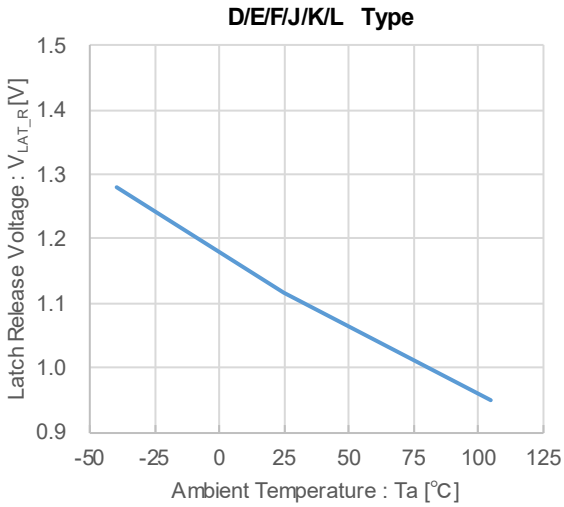
(21) Current Limit vs. Ambient Temperature



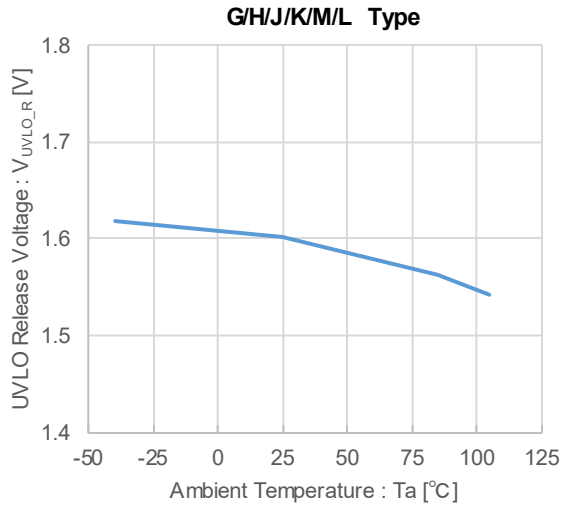
(22) Integral Latch Time vs. Ambient Temperature



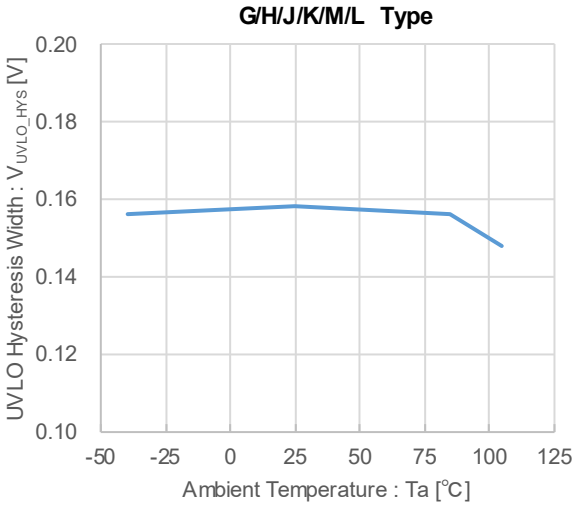
(23) Latch Release Voltage vs. Ambient Temperature



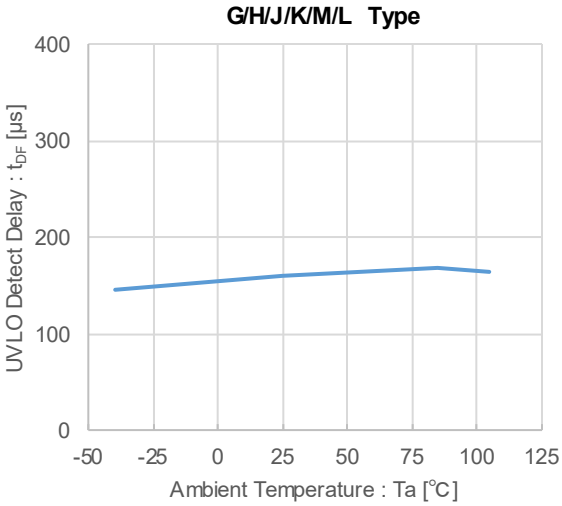
(24) UVLO Release Voltage vs. Ambient Temperature



(25) UVLO Hysteresis Voltage vs. Ambient Temperature



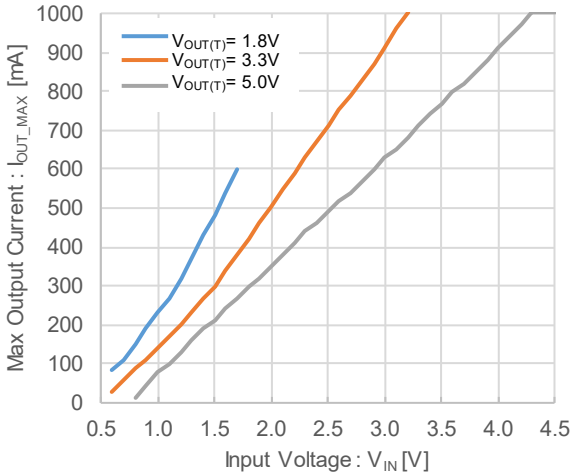
(26) UVLO Detect Delay vs. Ambient Temperature



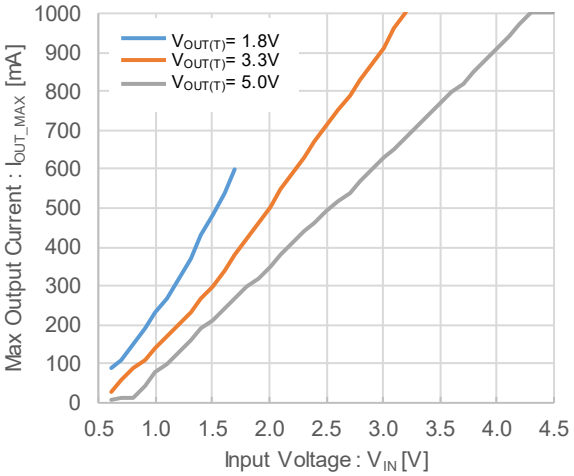
■TYPICAL PERFORMANCE CHARACTERISTICS

(27) MAX Output Current vs. Input Voltage

XCL104



XCL105

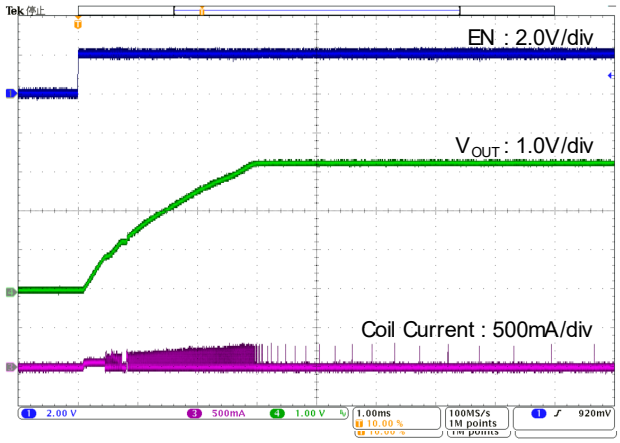


■TYPICAL PERFORMANCE CHARACTERISTICS

(28) Start-up Operation

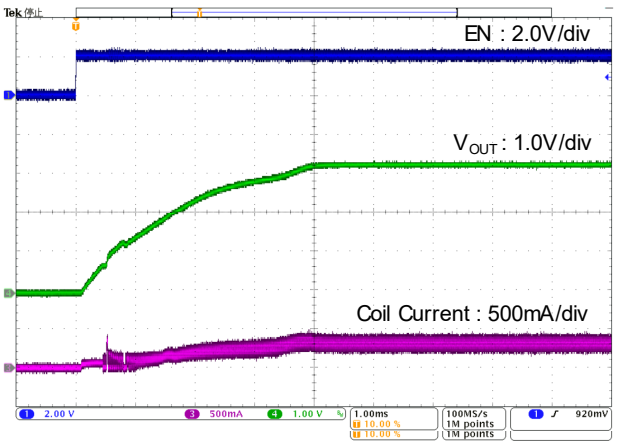
XCL105C33 ($V_{OUT(T)}$=3.3V)

V_{IN}=1.2V, $V_{OUT(T)}$=3.3V, RL=OPEN
C_{IN}=10μF (GRM188D71A106MA73)
C_L=30μF (GRM188D71A106MA73×3)



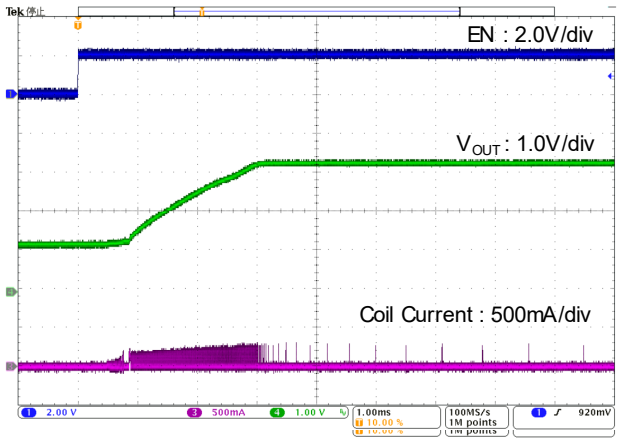
XCL105C33 ($V_{OUT(T)}$=3.3V)

V_{IN}=1.2V, $V_{OUT(T)}$=3.3V, RL=33Ω
C_{IN}=10μF (GRM188D71A106MA73)
C_L=30μF (GRM188D71A106MA73×3)



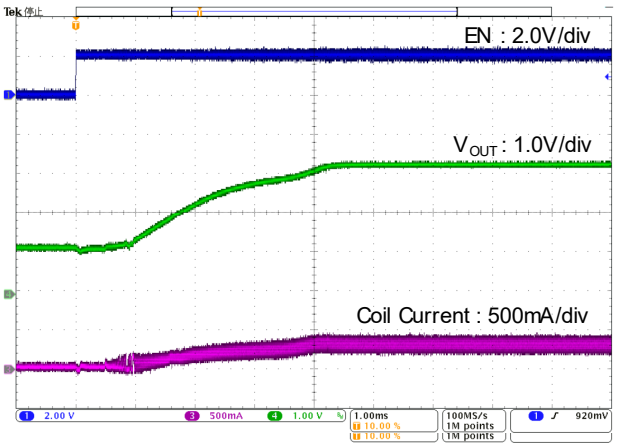
XCL105B33 ($V_{OUT(T)}$=3.3V)

V_{IN}=1.2V, $V_{OUT(T)}$=3.3V, RL=OPEN
C_{IN}=10μF (GRM188D71A106MA73)
C_L=30μF (GRM188D71A106MA73×3)



XCL105B33 ($V_{OUT(T)}$=3.3V)

V_{IN}=1.2V, $V_{OUT(T)}$=3.3V, RL=33Ω
C_{IN}=10μF (GRM188D71A106MA73)
C_L=30μF (GRM188D71A106MA73×3)

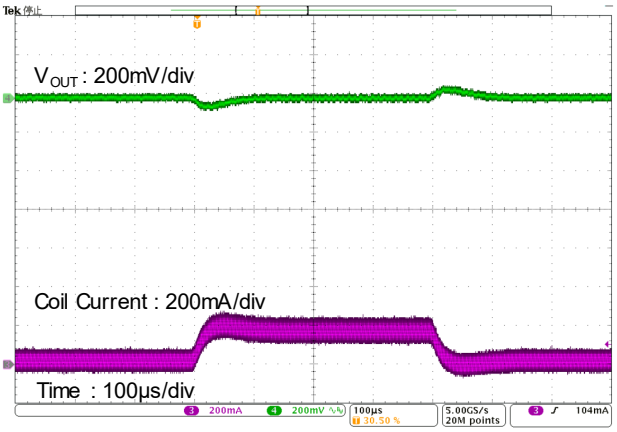


■TYPICAL PERFORMANCE CHARACTERISTICS

(29) Load Transient Response

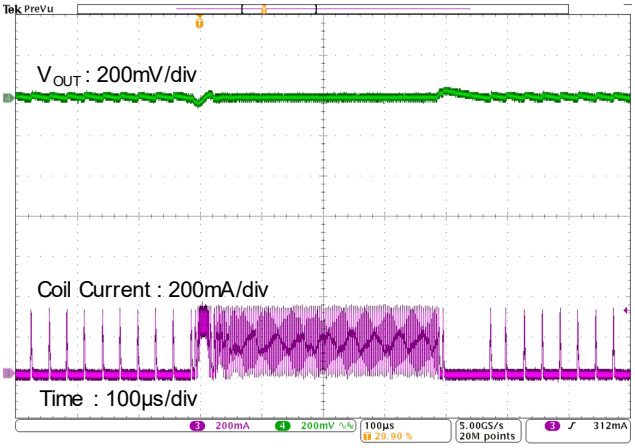
XCL104x18 ($V_{OUT(T)}$=1.8V)

V_{IN}=1.2V, $V_{OUT(T)}$=1.8V, I_{OUT}=10mA⇔100mA(tr=tf=1us)
C_{IN}=10μF (GRM188D71A106MA73)
C_L=30μF (GRM188D71A106MA73×3)



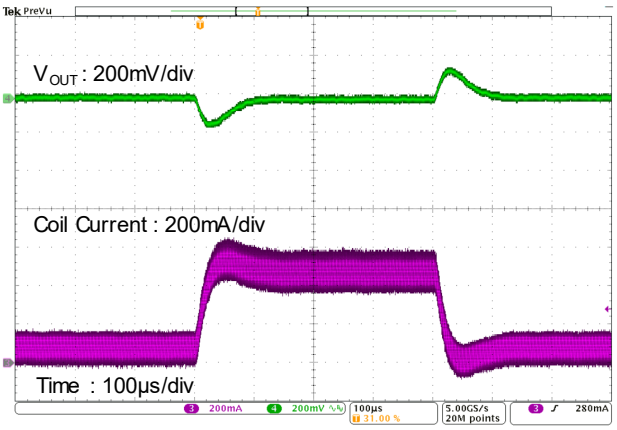
XCL105x18 ($V_{OUT(T)}$=1.8V)

V_{IN}=1.2V, $V_{OUT(T)}$=1.8V, I_{OUT}=10mA⇔100mA(tr=tf=1us)
C_{IN}=10μF (GRM188D71A106MA73)
C_L=30μF (GRM188D71A106MA73×3)



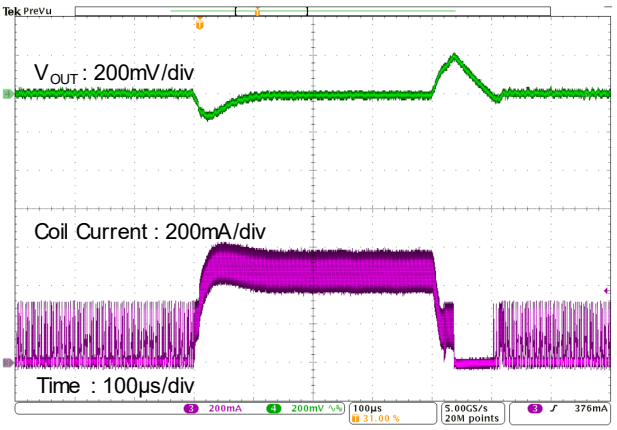
XCL104x33 ($V_{OUT(T)}$=3.3V)

V_{IN}=2.4V, $V_{OUT(T)}$=3.3V, I_{OUT}=50mA⇔300mA(tr=tf=1us)
C_{IN}=10μF (GRM188D71A106MA73)
C_L=30μF (GRM188D71A106MA73×3)



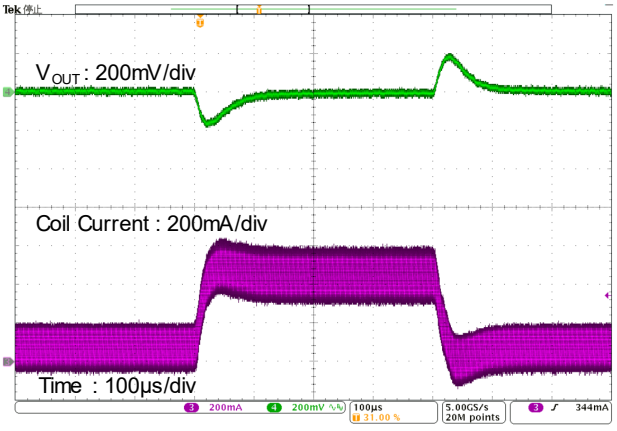
XCL105x33 ($V_{OUT(T)}$=3.3V)

V_{IN}=2.4V, $V_{OUT(T)}$=3.3V, I_{OUT}=50mA⇔300mA(tr=tf=1us)
C_{IN}=10μF (GRM188D71A106MA73)
C_L=30μF (GRM188D71A106MA73×3)



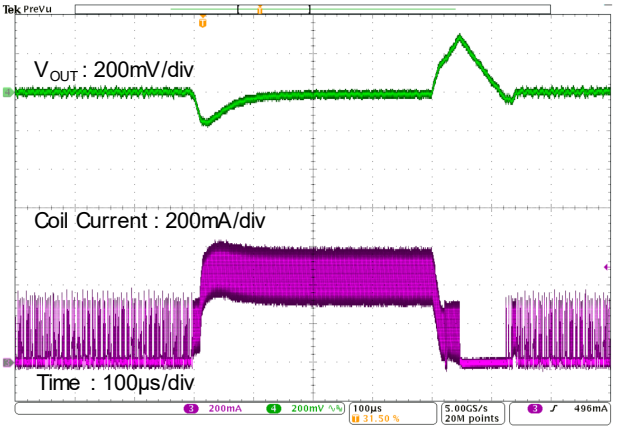
XCL104x50 ($V_{OUT(T)}$=5.0V)

V_{IN}=3.7V, $V_{OUT(T)}$=5.0V, I_{OUT}=50mA⇔300mA(tr=tf=1us)
C_{IN}=10μF (GRM188D71A106MA73)
C_L=30μF (GRM188D71A106MA73×3)



XCL105x50 ($V_{OUT(T)}$=5.0V)

V_{IN}=3.7V, $V_{OUT(T)}$=5.0V, I_{OUT}=50mA⇔300mA(tr=tf=1us)
C_{IN}=10μF (GRM188D71A106MA73)
C_L=30μF (GRM188D71A106MA73×3)



■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
DFN3030-10B	DFN3030-10B PKG	DFN3030-10B Power Dissipation

■MARKING RULE

■DFN3030-10B

MARK① represents product series and Oscillation Frequency

MARK	PRODUCT NUMBER	TYPE	OUTPUT VOLTAGE RANGE	PRODUCT SERIES
0	XCL104	A	1.8～3.6V	XCL104A181H2-G～XCL104A361H2-G
1			3.7～5.5V	XCL104A371H2-G～XCL104A551H2-G
2		D	2.2～3.6V	XCL104D221H2-G～XCL104D361H2-G
3			3.7～5.5V	XCL104D371H2-G～XCL104D551H2-G
C		G	2.2～3.6V	XCL104G221H2-G～XCL104G361H2-G
D			3.7～5.5V	XCL104G371H2-G～XCL104G551H2-G
E		J	2.2～3.6V	XCL104J221H2-G～XCL104J361H2-G
F			3.7～5.5V	XCL104J371H2-G～XCL104J551H2-G
4	XCL105	A	1.8～3.6V	XCL105A181H2-G～XCL105A361H2-G
5			3.7～5.5V	XCL105A371H2-G～XCL105A551H2-G
6		B	1.8～3.6V	XCL105B181H2-G～XCL105B361H2-G
7			3.7～5.5V	XCL105B371H2-G～XCL105B551H2-G
8		C	1.8～3.6V	XCL105C181H2-G～XCL105C361H2-G
9			3.7～5.5V	XCL105C371H2-G～XCL105C551H2-G
A		D	2.2～3.6V	XCL105D221H2-G～XCL105D361H2-G
B			3.7～5.5V	XCL105D371H2-G～XCL105D551H2-G
H		E	2.2～3.6V	XCL105E221H2-G～XCL105E361H2-G
K			3.7～5.5V	XCL105E371H2-G～XCL105E551H2-G
L		F	2.2～3.6V	XCL105F221H2-G～XCL105F361H2-G
M			3.7～5.5V	XCL105F371H2-G～XCL105F551H2-G
N		G	2.2～3.6V	XCL105G221H2-G～XCL105G361H2-G
P			3.7～5.5V	XCL105G371H2-G～XCL105G551H2-G
R		H	2.2～3.6V	XCL105H221H2-G～XCL105H361H2-G
S			3.7～5.5V	XCL105H371H2-G～XCL105H551H2-G
T		M	2.2～3.6V	XCL105M221H2-G～XCL105M361H2-G
U			3.7～5.5V	XCL105M371H2-G～XCL105M551H2-G
V		J	2.2～3.6V	XCL105J221H2-G～XCL105J361H2-G
X			3.7～5.5V	XCL105J371H2-G～XCL105J551H2-G
Y		K	2.2～3.6V	XCL105K221H2-G～XCL105K361H2-G
Z			3.7～5.5V	XCL105K371H2-G～XCL105K551H2-G
C		L	2.2～3.0V	XCL105L221H2-G～XCL105L301H2-G
D			3.1～3.9V	XCL105L311H2-G～XCL105L391H2-G
E			4.0～4.8V	XCL105L401H2-G～XCL105L481H2-G
F			4.9～5.5V	XCL105L491H2-G～XCL105L551H2-G

■MARKING RULE

MARK② represents output voltage

・XCL104, XCL105A/B/C/D/E/F/G/H/M/J/K

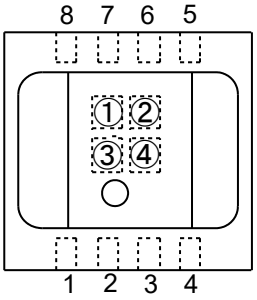
MARK	OUTPUT VOLTAGE RANGE		MARK	OUTPUT VOLTAGE RANGE	
0	1.8	3.7	A	2.8	4.7
1	1.9	3.8	B	2.9	4.8
2	2.0	3.9	C	3.0	4.9
3	2.1	4.0	D	3.1	5.0
4	2.2	4.1	E	3.2	5.1
5	2.3	4.2	F	3.3	5.2
6	2.4	4.3	H	3.4	5.3
7	2.5	4.4	K	3.5	5.4
8	2.6	4.5	L	3.6	5.5
9	2.7	4.6			

・XCL105L

MARK	OUTPUT VOLTAGE RANGE			
M	2.2	3.1	4.0	4.9
N	2.3	3.2	4.1	5.0
P	2.4	3.3	4.2	5.1
R	2.5	3.4	4.3	5.2
S	2.6	3.5	4.4	5.3
T	2.7	3.6	4.5	5.4
U	2.8	3.7	4.6	5.5
V	2.9	3.8	4.7	
X	3.0	3.9	4.8	

MARK③,④ represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order.
(G, I, J, O, Q, W excluded. No character inversion used.)

DFN3030-10B



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